SZPL3102A/3103A-C

High Voltage, High Efficiency 65W Buck Converter

Features

- Selectable Switching Frequency up to 2 MHz
- Optimal High Efficiencies for 3.3 V to 21 V Vout
- Maximum Output Current of 3.25 A
- Wide Input Voltage Range: 7 V to 27 V
- Selectable Soft Start Times
- OCP/OVP/OTP Protections
- Programmable UVLO
- 3 mm x 3 mm QFN Package

Applications

- VBUS Supply Generation for USB-PD Ports:
  - Multiple Output USB-PD Chargers
  - Charging Hubs
  - Displays and Televisions
  - Laptop Docking Stations
- High Voltage POL Supplies

Product Description

The SZPL3102A is a fully integrated high efficiency synchronous buck DC/DC converter intended to be paired with certain USB-PD Controllers having their own feedback resistor divider. The SZPL3103A is different in that it requires an external feedback divider. Both devices are optimized for the highest efficiency performance, including dual input LDOs for self-bias, across a wide output voltage range.

The SZPL3102A is designed to supply the full range VBUS rail for USB-PD ports and can be controlled by popular USB-PD controllers or fast charging devices. On start-up, the device employs an internal feedback path to allow safe regulation until the external PD controller powers up and becomes available to regulate the output voltage. Following this initial start-up period, the SZPL3102A hands over output control to the external PD controller. The SZPL3103A feedback exclusively uses an external discrete resistor divider for output voltage regulation.

The SZPL3102A and SZPL3103A are available in a compact 3 mm x 3 mm custom QFN package, delivering high power density with a minimal number of external components.

Application Diagram

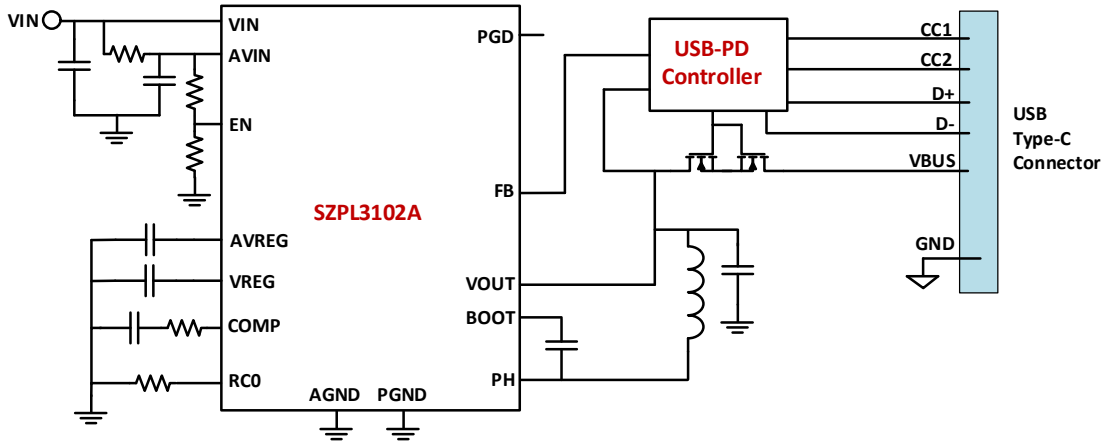

Figure 1. Typical SZPL3102A USB-PD Port Application Diagram

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Package Pinout

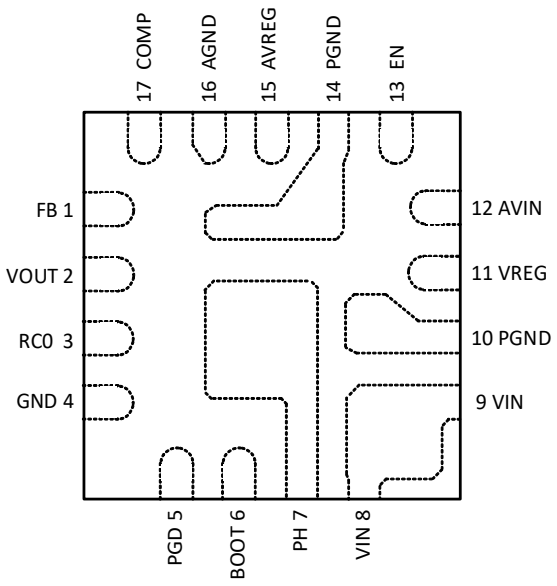


Figure 2. Package Pinout - Top View

Pin Definitions

Pin #	Name	Description
1	FB	Feedback input pin, nominally regulated to 1.25 V. For SZPL3102A: connect to the tap of a VOUT-to-AGND resistor divider network and the analog feedback control output of PD controller. For SZPL3103A: connect to the tap of external VOUT-to-AGND resistor divider network.
2	VOUT	Voltage sense line from regulated output of converter and secondary input to internal LDOs.
3	RC0	Analog input. A resistor to ground sets switching frequency (F_{SW}) and soft start time (t_{SS}).
4	GND	Connect to ground.
5	PGD	Power good output signal. Active high, open drain output. Connect to pullup resistor to VREG.
6	BOOT	Bootstrap high side driver voltage supply. Connect to 0.1 uF capacitor to PH node.
7	PH	Phase (switch) node of the buck converter's output FETs. Connect to output inductor.
8, 9	VIN	Input voltage to the buck converter's output FETs (high side drain). Locally decouple with 1 uF + 0.1 uF capacitors, followed by enough capacitors to provide the required input RMS current.
10	PGND	Power ground connection of output FETs (low side source). Connect to ground.
11	VREG	Internal 3.3 V LDO output. Connect to a 1 uF bypass capacitor to ground.
12	AVIN	Input voltage to the buck converter for analog circuits. Connect to tap of VIN RC low-pass filter.
13	EN	Analog control input. A potential higher than the UVLO threshold enables switching operation and output soft start process. A potential lower than the shutdown threshold places the device in a low power state. Decouple with one 1 nF to 100 nF capacitor placed close to the part. See the Functional Description paragraph for a more detailed explanation of operation.
14	PGND	Connect to ground.
15	AVREG	Internal 3.3 V LDO output. Connect a 1 uF bypass capacitor to ground.
16	AGND	Connect to ground.
17	COMP	Compensation error amplifier output. Connect to a RC network to ground. See the Applications Information section for recommendations.

Functional Block Diagram

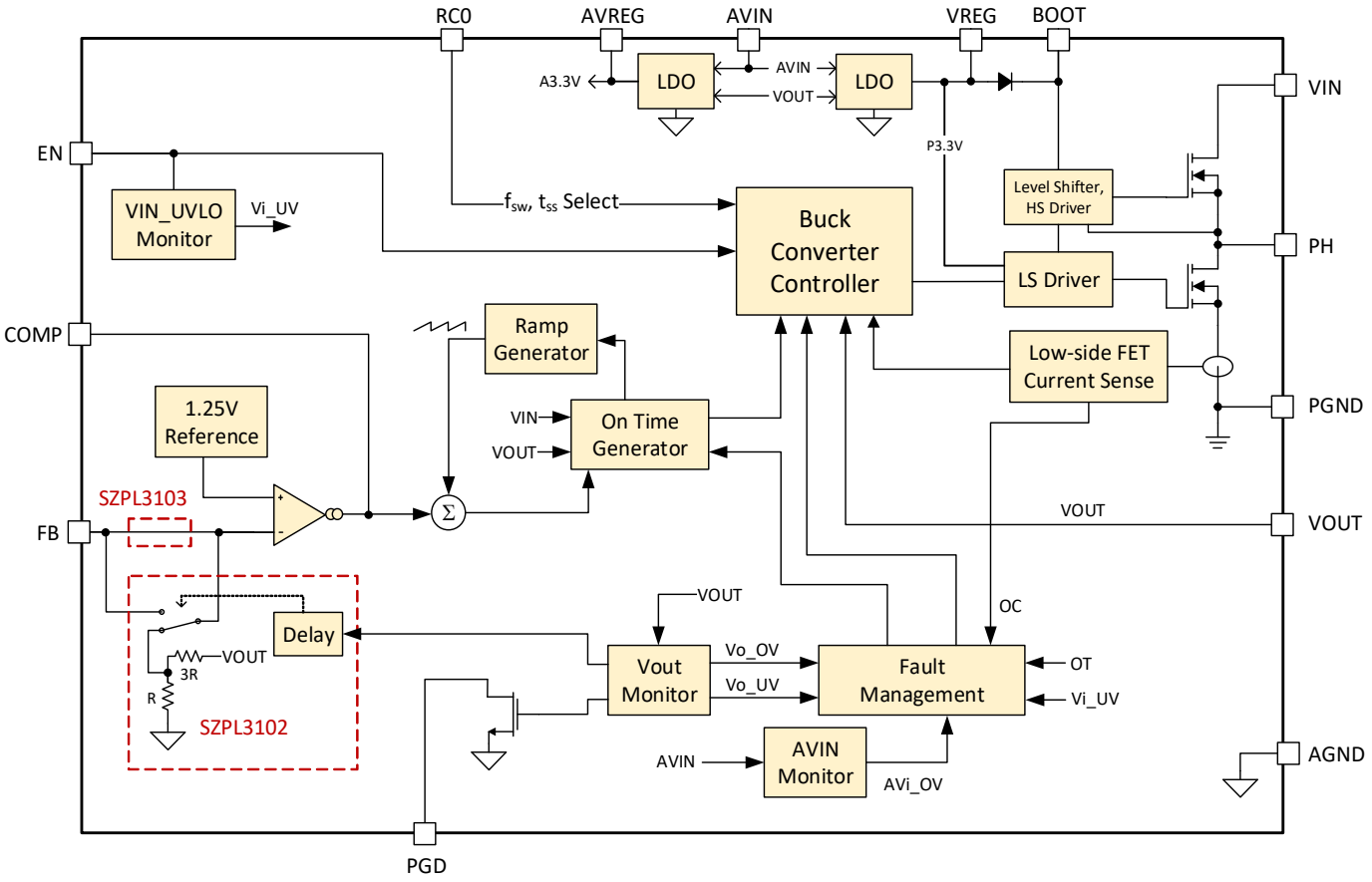


Figure 3. Functional Block Diagram

Absolute Maximum Ratings

(Ta = 25 °C Unless Otherwise Specified.) (1)

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage (DC)	V_{AVIN}, V_{VIN}, V_{VOUT}	Relative to PGND	-0.3	28	V
V_{PH} (AC, <10 ns)	V_{PH}	Relative to PGND	-2	35	
I/O Pins	V_{EN}, V_{PGD}, V_{COMP}, V_{FB}, V_{RC0}	Relative to AGND	-0.3	6	
Storage Temperature Range	T_{STG}		-50	150	
Junction Temperature	T_J		-40	150	°C

Notes:

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Thermal Information

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient (1)(2)	$R_{\Theta JA}$		28.2		°C/W
Thermal Resistance Junction to Top of Package (2)	$R_{\Theta JC(TOP)}$		16.6		
Thermal Resistance Junction to Board (2)	$R_{\Theta JB}$		4.9		
Thermal Characterization Parameter - Junction to top (2)	Ψ_{JT-TOP}		1.2		
Thermal Characterization Parameter – Junction to bottom case (2)	Ψ_{JC-BOT}		2.0		
Thermal Characterization Parameter - Junction to board (2)	Ψ_{JB}		4.9		

Notes:

1) 4-Layer JEDEC PCB with 12 thermal vias as per specification JESD51-5.
2) Based upon simulations; I_{OUT} = 3.25A.

Recommended Operating Conditions

(Ta = 25°C Unless Otherwise Specified.) (1)

Parameter	Symbol	Conditions	Min.	Max.	Units
Power Stage Input Supply Voltage (2)	V_{AVIN}, V_{VIN}	Relative to PGND	7	27	V
Output Current	I_{OUT-DC}	DC, Continuous		3.25	A
Operating Junction Temperature	T_J		-40	125	°C

Notes:

1) Device functionality is not guaranteed outside the recommended operating conditions.
2) Attention to proper VIN and AVIN pins input supply bypassing and tight PCB layout must be observed to keep the peak voltage of any ringing on the phase node, at the PH pins, below the Absolute Maximum Ratings above.

Electrical Characteristics

Unless otherwise noted, VIN = 24 V, F_{SW} = 1.00 MHz, I_{LOAD}=0, COUT = 50 µF, LOUT = 3.3uH, T_J = -40 °C to 125 °C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Input Power Supply						
Supply Current (shutdown)	I_{AVIN_SD}	V_{EN}=0 V		25	35	µA
	I_{VIN_SD}				10	
Supply Current (UVLO)	I_{AVIN_UVLO}	$V_{EN\_SDH} < V_{EN} < (V_{EN\_UVLO} - V_{EN\_UVLOhys})$, V_{OUT} = 0		1,400	1,600	µA
	I_{VIN_UVLO}				10	
VIN Supply Current (Operating)	I_{IN}	VOUT=5V, I_{LOAD}=0, V_{EN}> V_{EN_UVLO}; Fsw=0.67 MHz to 2 MHz		2.1		mA
Switching Operation						
Switching Frequency, CCM operation	F_{sw}	312 kΩ ≤ R_{RC0} ≤ 723 kΩ, T_A = 25 °C, V_{OUT} = 5V		667		kHz
		81.6 kΩ ≤ R_{RC0} ≤ 240 kΩ, T_A = 25 °C, V_{OUT} = 5V		1,000		
		22.3 kΩ ≤ R_{RC0} ≤ 51.7 kΩ, T_A = 25 °C, V_{OUT} = 5V		1,667		
		5.8 kΩ ≤ R_{RC0} ≤ 17.1 kΩ, T_A = 25 °C, V_{OUT} = 5V		2,000		
Minimum ON Time	T_{ON_MIN}	Note 1		26		ns
Minimum OFF Time	T_{OFF_MIN}	Note 1		70		ns
Protection						
Output Under-Voltage (UVP)	V_{OUT_UVP}			80		%
Output UVP Hysteresis	V_{OUT_hys}			5		%
Output Current Limit (OCP)	I_{LIM}		3.6	4.0		A
Thermal Shutdown (OTP)	T_{SD}	Note 1		150		°C
Thermal Shutdown Hysteresis	T_{HYS}	Note 1		20		°C
Input Over Voltage	V_{AVIN_OVP}			28		V
Input Over Voltage Hysteresis	V_{AVIN_OVPhys}			0.2		V
Output Protection UVP/OCP/OTP, Input OVP, Hiccup Delay	t_{VOUT_PDLY}	Following a cleared fault condition		32		ms
Protection Soft-Start Delay	t_{DLY}			40		% of t_{SS}
Reference and Soft-Start						
Feedback Voltage	V_{REF}	V_{REF}, as regulated at FB pin	1.225	1.250	1.275	V
Soft-Start Time Accuracy	t_{SS}	Nominal value selectable by R_{RC0}	-30		+30	%
Enable Logic Input						
EN shutdown threshold	V_{EN_SDH}		0.62	0.72	0.82	V
EN shutdown threshold hysteresis	V_{EN_SDhys}			130		mV
EN UVLO threshold	V_{EN_UVLO}	AVIN > ~4.5V	1.200	1.280	1.350	V
EN UVLO threshold hysteresis	$V_{EN\_UVLOhys}$	AVIN > ~4.5V		130		mV
EN UVLO Hiccup Delay	$V_{EN\_UVLOdly}$			1		ms
EN input bias current	I_{EN_IN}	V_{EN} = 1.5 V		10		nA

Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
LDO Voltages						
Internal VREG LDO	V_{VREG}			3.40		V
Internal AVREG LDO	V_{AVREG}			3.30		V
FB Input Pin						
FB input bias current	I_{FB_IN}	V_{FB} = 1.25 V		1	50	nA
Power Good						
PGD Assert Threshold	$PGD_{th\_hi\_R}$	V_{FB} rising		90		% of V_{FB}
	$PGD_{th\_hi\_F}$	V_{FB} falling		110		
PGD De-assert Threshold	$PGD_{th\_lo\_R}$	V_{FB} rising		115		
	$PGD_{th\_lo\_F}$	V_{FB} falling		85		
PGD Startup Delay	PGD_{TD}	V_{FB} rising		40		% of t_{SS}
PGD Assert Delay	PGD_{ATD}	V_{FB} rising		8		µs
PGD De-assert Delay	PGD_{DTD}	V_{FB} falling		2		µs
PGD Low Drive	V_{OL_PGD}	I_{PGD} = 10 mA; EN > V_{EN_UVLO}			0.4	V
PGD High Leakage	I_{LK_PGD}	V_{PGD} = 3.3 V			1	µA

Notes:

1) Parameter is guaranteed by design and characterization and is not tested in production.

Functional Description

General

The SZPL3102A/3103A is a high-performance point of load DC/DC converter. While operating in constant conduction mode (CCM), the controller uses a constant-on-time architecture that compensates for input and output variations to keep the switching frequency relatively constant. Automatic switch-over to discontinuous conduction mode (DCM) improves efficiency under extended light-load operation.

Protection features include an externally adjustable under-voltage lockout (UVLO) via the threshold-sensitive EN pin, integrated over-temperature (OTP), output overcurrent (OCP), as well as output under-voltage (UVP).

Initialization and EN Pin Operation

With the EN pin held below its shutdown threshold, the device is disabled and held in a low power mode designed to preserve energy. The internal circuitry is initialized once the SZPL3102A/3103A has sufficient bias for the internal LDOs to be functional (AVIN > ~4.5 V), and the EN pin is higher than its shutdown threshold (EN > V_{EN_SDH}). Various operating parameters are set during the initialization, and the part is readied for switching operation. The sequence may last ~1.3 ms and could be immaterial to the operation of the circuit should EN take longer to transition between its shutdown and UVLO thresholds. Should the EN pin transition swiftly from the shutdown disabled state to UVLO enabled state, switching operation is delayed by this initialization phase of the device's operation.

Following initialization, once the EN pin voltage exceeds its UVLO threshold, the device immediately begins switching operation, ramping up the output voltage in a linear, controlled fashion. A subsequent EN crossing above the UVLO threshold following a successful startup sequence results in switching operation being delayed by ~1 ms.

An input supply UVLO can be implemented above AVIN's minimum operating voltage using a resistor divider and the controller EN pin's UVLO threshold.

Startup

Following initialization and with all other conditions for operation met, the SZPL3102A/3103A commences switching operation and output voltage ramp-up (soft-start). Switching operation commences with sixty-four 50 ns, ~1.1 MHz lower switch ON cycles, designed to ensure the BOOT capacitor is fully charged up. The first 32 of these cycles are softer, reduced dV/dt cycles. Following the BOOT capacitor charging period, startup operation continues as dictated by the circuit settings and operating conditions.

The SZPL3102A/3103A can start up into a pre-biased output (V_{OUT} > 0). The output (PH) remains tri-stated until the reference exceeds the FB voltage, at which point CCM switching is initiated. Exceptions to tri-state are 50ns BOOT refresh lower switch ON cycles, generated every ~20 µs.

Switching Frequency and Soft Start Time Selection, Forced CCM Operation

The operating switching frequency and output voltage ramp-up (soft-start) time are both set by an external resistor connected between the RC0 pin and AGND, R_{RC0}. Once the SZPL3102A/3103A exits quiescent state, internal circuitry 'reads' the value of this resistor and internally sets the switching frequency and soft-start period, as detailed in Table 1. Select the indicated RC0 resistor value that matches the desired available combination of switching frequency and soft-start period. These operating parameters, once set, are latched until the device loses its bias supply (AVIN) or is otherwise disabled to a shutdown state (EN < V_{EN_SDH}). One percent accuracy or better resistors (E96 series) should be used.

At any time while the device is operational, outside of the initialization phase, bringing the RC0 pin potential to ground (<~50 mV) forces the circuit into CCM operation.

Table 1: Switching Frequency Resistor Values-RC0 Pin

RC0 (kΩ)		tss (ms) 1	2	4	8
Fsw (MHz)	0.67	715	549	422	316
	1.0	237	169	121	82.5
	1.67	51.1	39.2	30.1	22.6
	2.0	16.9	12.1	8.66	5.9

Switching Operation, Auto-DCM and Ultrasonic Limit

The SZPL3102A/3103A ramps up the output voltage operating in CCM. Following the output soft-start period and anytime during normal operation, the device will switch into DCM after 64 consecutive switching cycles of the inductor ripple crossing into the negative domain. DCM operation switching frequency is determined by the load magnitude and other circuit parameters (V_{IN}, V_{OUT}, L_{OUT}, etc.). Operation in DCM improves the circuit's light load efficiency. DCM entry is not possible should the lower FET conduction time be shorter than the negative current sensing blanking time.

While in DCM operation, the switching frequency is bound by a ~50 kHz lower limit (ultra-sonic operation). This lower limit ensures the BOOT capacitor can be periodically refreshed and prevents possible audible emissions from the circuit elements. A DCM cycle features an upper switch ON pulse larger than the corresponding CCM duration, followed by a lower switch ON period, terminated when the inductor current crosses below 0 A. An ultrasonic DCM cycle begins with a brief lower switch ON period designed to refresh the BOOT capacitor, followed by the DCM cycle described above. A DCM cycle is triggered either by the error amplifier output or forced by the ultrasonic timeout generator.

Over-Current, Under-Voltage, Over-Voltage and Over-Temperature Protection

The SZPL3102A/3103A features a comprehensive list of protection features. Output Under-Voltage (UV) protection is based upon the output voltage level sensed at the FB node. Over-Current (OC) is implemented by sensing the low-side power switch current (PH node voltage drop) at the end of its conduction period. Input Over-Voltage (OV) senses the input voltage at the AVIN pins.

OC protection prevents another high side power switch ON pulse while the sensed current is above the over-current threshold (I_{LIM}). The result is a cycle-by-cycle inductor valley current limit. The actual converter average output current in this mode of operation is dependent on the amount of ripple current. If the inductor current does not decay to a level below the over-current threshold before the modulator calls for another high-side pulse, the start of the high side switch ON-time is delayed, resulting in an output current smaller than the load current. Should the converter not be able to deliver the full load current, its output voltage will begin to sag below the regulation setpoint. If the output voltage falls to the under-voltage threshold (V_{UVP}), or when 16 consecutive cycles of over-current are detected, an OC fault is asserted, and PGD is de-asserted.

OC protection is also implemented for the negative inductor current domain. Should the output tend to rise above the regulated setpoint, the SZPL3102A/3103A will attempt to correct the deviation, by sinking current from the output. Circuit response to such a situation is dependent on the operating mode, whether in DCM or CCM operation, when the deviation is detected. In DCM operation, if the output voltage rises above the regulation setpoint, the circuit remains in ultra-sonic mode, but the effective duty cycle decreases, sinking current from the output up to the negative inductor valley threshold. Similarly, while in CCM operation, the circuit also operates as a boost converter, sinking current from the output up to the negative valley threshold and boosting the input. The negative current operation is limited by a cycle-by-cycle negative OCP threshold of ~60 % of the positive inductor current OCP limit. Negative current sensing is blanked for the first ~100 ns of the lower FET conduction period.

Output UV is asserted following a ~8 μs delay from threshold cross. Output UV condition is ignored while PGOOD reporting is not active (see Power Good Operation). Input OV is asserted upon VIN exceeding V_{AVIN_OVP} and de-asserted upon it falling below the level determined by V_{AVIN_OVPhys}. Circuit operation is immediately suspended upon reaching Over-Temperature (OT) threshold (T_{SD}) and allowed to resume as it clears the temperature hysteresis (T_{HYS}). Upon the assertion of any (OC, UV, OV, OT) fault condition, the inductor current is first returned to 0, then the output (PH) is tri-stated.

Should all conditions for operation still be met upon clearing a particular fault, the SZPL3102A/3103A resumes operation, attempting an output soft-start after expiration of the applicable hiccup interval.

Power Good (PGD) Operation

The PGD pin monitors and reports the controlled output voltage status, as sensed at the FB pin. Following an initial output voltage soft-start period, PGD reporting is delayed by a time interval ~40 % of the soft-start interval, t_{SS}. Additionally, to prevent chatter, every assertion of PGD is blanked by PGD_{ATD} time duration and every de-assertion by PGD_{DTD} time duration. PGD signal is de-asserted

immediately following the onset of a fault and re-asserted again following a successful output voltage soft-start.

Integrated Bias LDOs Operation

The SZPL3102A/3103A feature two dual-input low drop-out linear regulators (LDOs). One is designed to power the analog circuitry (AVREG), while the other is powering the power stage drivers (VREG). Both LDOs derive their output from AVIN as the input and switch over to VOUT as the input when its amplitude exceeds ~4.5 V.

Operation with USB-PD and QC Controllers

The SZPL3102A/03A can be used to supply the VBUS voltage rail for USB charging ports or hubs. The device can interface directly with a selection of different USB-PD controllers and other fast charging devices. Some of such compatible devices are listed below, though many others may be available for pairing.

USB-PD controllers:

- Weltrend WT6633P (SZPL3102A)
- Cypress CCG3PA (SZPL3103A)

Fast Charging Devices:

- Power Integrations CHY103 (SZPL3103A)

The SZPL3102A is intended for use with USB controllers that feature disconnectable internal resistor dividers for setting the output voltage, such as WT6633P. The SZPL3102A uses its internal FB resistor divider (refer to Figure 3) to ramp up the output voltage and provide bias to the USB controller, allowing it time to connect its own divider into the circuit. The SZPL3102A disconnects its internal divider when the output voltage exceeds ~4 V, ceding control of the DC output voltage level to the USB controller.

The SZPL3103A requires an external resistor divider for setting the DC output voltage.

Layout Considerations

Switch-mode DC/DC converters owe their popularity in large part to their efficient operation, which is primarily affected by their switching speed, defined as the speed of current commutation between the output power switches. An optimal layout will best manage the challenges associated with fast current and voltage transitions while providing adequate power and heat dissipation into the surrounding environment.

Generally, the physical implementation of the circuit yields both sources of noise, as well as receptors for the generated noise. The goal is to primarily minimize the sources' amplitudes, or ability to generate noise, and minimize the pick-up of noise by sensitive receptors.

Transmission of switching noise can also be mitigated by reducing the coupling between sources and receptors, which should be a closely ranked secondary goal.

A current switched at a fast rate of change generates proportional voltage spikes across inductive circuit elements and magnetic field changes in the conductors carrying the commutated current. To help control noise propagation, minimize the inductance in the path of commutated current and magnetic coupling between such conductors. In a complementary fashion, a circuit node whose voltage potential changes rapidly effects a proportional change in the electric field it generates. Sudden changes in potential can propagate capacitively into receptive surrounding circuit nodes. Minimizing the capacitive parasitic circuit elements between such nodes is highly desirable.

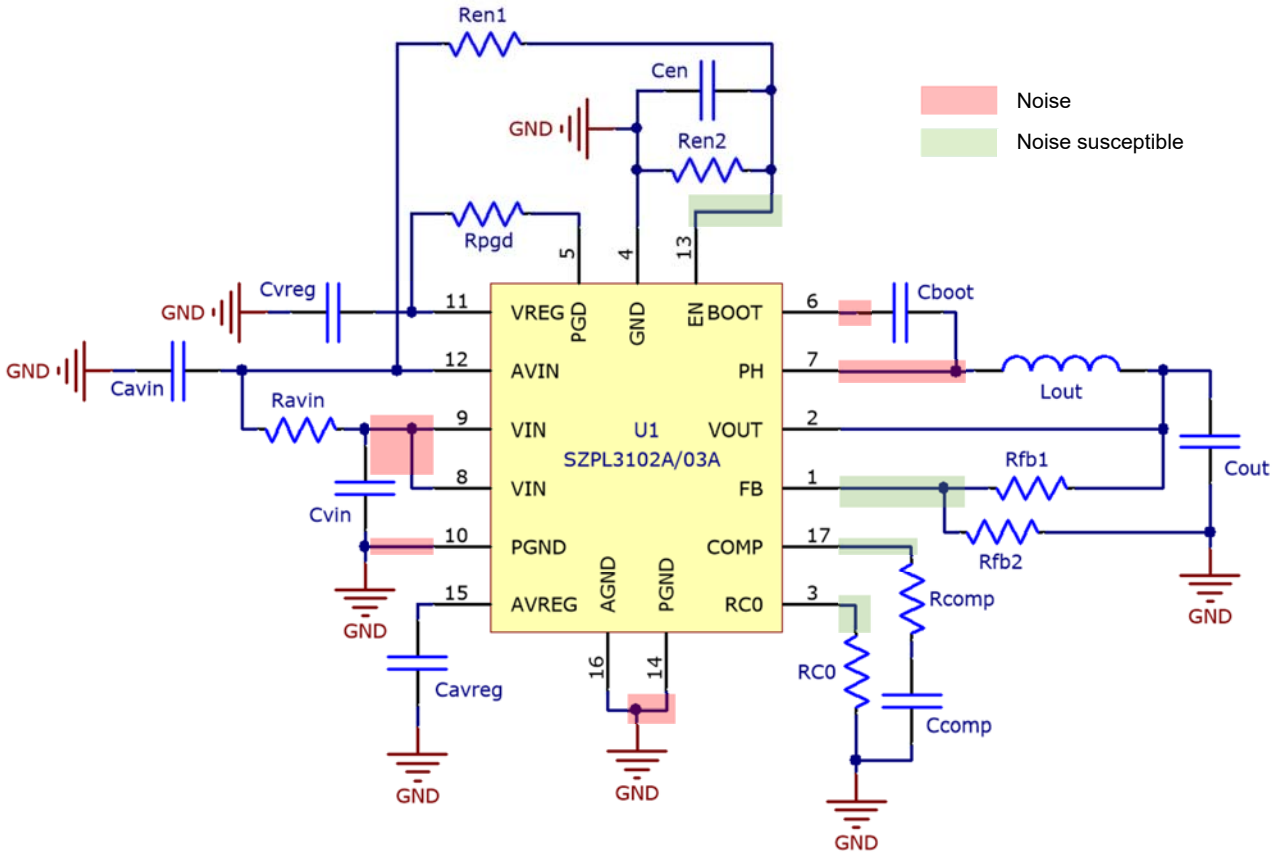


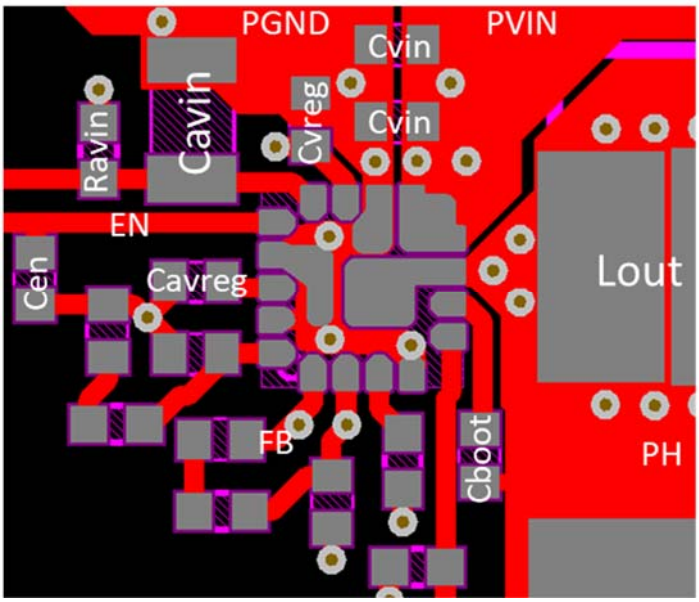
Figure 4. Layout Considerations

Figure 4 highlights the typical circuit nodes that can be identified as sources or receptors of switching noise. Utilize the following guidelines when laying out a printed circuit board employing an SZPL3102A/03A device:

- For the lowest inductance connections to ground, dedicate one PCB layer to this circuit node and perform all connections to it using the shortest available path, typically a via placed in or near the respective component terminal pad.

Figure 5. Example PCB Layout – Top Side Placement and Routing

- Create a pad under the SZPL3102A/03A's package, similar to that shown in Figure 5, that connects all the device's ground pins (GND, AGND, PGND) together. Tie the pad itself to the ground plane using solder resist covered vias under the package.



- Fan out the PH, PGND, and VIN peripheral device pads to wide top layer islands. This will improve heat transfer and reduce the interconnect parasitics to power path decoupling capacitors.

- Place power path decoupling as close as practicable to the device's power pins; smallest (least inductive) packages should be placed closest to the device.

- Use a few vias placed on the PH, VIN and PGND islands, close to the device, to help conduct the generated heat to planes/islands on other layers and reduce the interconnect parasitics.

- In a typical 4-layer implementation, to minimize PH node local capacitive coupling to the ground (typically 2nd layer in the stack-up), carve out an identical island in the second layer pour.

- The sensitive, small signal, high impedance nodes (FB, EN) are routed *away* from the power switching connections using optimized-length connections. These sensitive traces do not share or overlap any of the power conduction paths.

If (micro) vias-in-pad are feasible, they can greatly reduce the device's thermal impedance, more so if using copper filled and plated vias. For via usage, use smaller, more densely packed vias rather than fewer larger ones. This approach leads to better copper utilization, by reducing effective inductance and local current density in the copper of the penetrated layers.

Application Design Guide

The design guide is intended to provide a high-level overview of some of the steps necessary to create a complete DC/DC converter circuit. Various aspects are covered individually and in the context of listed assumptions.

Selection of Bypass/Decoupling Capacitors

The input bypass capacitors must provide a low impedance at high frequency between the VIN and the PGND pads. Use a small form factor, small value capacitor as close as possible to the VIN and PGND pins. A 100 nF to 1 μF capacitor in a 0402 (up to 0603) package is ideal. Located next to this small form factor decoupling capacitor, provide enough bulk capacitance to meet the input RMS current at full output load.

$$I_{IN(RMS)} = \sqrt{I_{OUT}^2 \cdot (D - D^2) + I_{L,P-P}^2 \cdot \frac{D}{12}} \quad (1)$$

Where:

- I_{OUT} is the full output load current
- $I_{L,\,P\text{-}P}$ is the inductor peak-peak ripple current

- D is the PWM duty cycle

For designs where the output voltage can vary over a wide range, pick the worst-case situation, which can be approximated as 50 % of I_{OUT}, occurring at D = 0.5 (50%). Figure 6 offers a graphical option to approximating the input RMS current for a selection of output inductor ripple values over the full range of the PWM duty cycle. Should the application ever have to actively slow down the output, check the ability of the input supply to sink current. If the input supply is unable to sink the input current caused by the boost operation of the circuit, additional input bulk capacitance may be required to absorb the charge transferred from the output of the circuit and limit the input-side voltage rise to a safe level.

Ceramic bulk capacitor technology is recommended for the input RMS bypass. Select components with X5R, X7R, similar or better dielectric, and consider the voltage rating to avoid excessive capacitance loss due to DC bias. Where required, electrolytic or polymer capacitors with suitably low ESR/ESL can be used to supplant or replace the higher capacitance bulk ceramic components.

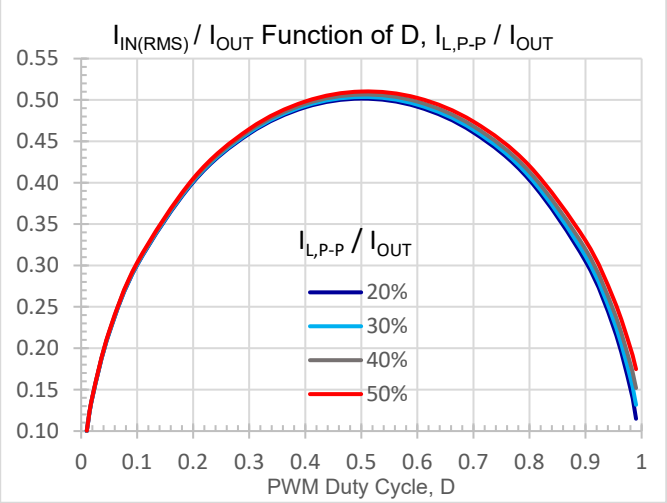


Figure 6: Input RMS Current

Each of the AVIN, AVREG, and VREG pins of the SZPL3102A/3103A device should be decoupled with at least 1 µF of effective ceramic capacitance in small form factor, placed as close as practicable to the respective pins of the device. Select appropriate dielectric and voltage rating capacitors, paying attention to DC bias derating.

Selection of Output Inductor

The output inductor should be chosen so that the ripple current is not excessive and so that the desired output current will not cause overheating or core saturation. Typically, the amount of ripple current is chosen in the 20 % to 40 % of the expected full load current. The required inductance is:

$$L = \frac{V_{OUT}}{V_{IN}} \cdot \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot I_{P-P}} \qquad (2)$$

Where:

- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- F_{SW} is the switching frequency
- I_{P-P} is the peak to peak inductor ripple

In situations where the input or the output voltages can vary during operation of the circuit, take into consideration the worst-case conditions.

Selection of Output Capacitors

The output capacitors filter the PWM converter output, absorbing the output inductor ripple current. They also buffer load transients, providing charge following the application of the load, while the inductor current is ramping up. They also absorb the output inductor stored energy following load removal. Multi-layer ceramic capacitors (MLCCs) are recommended to achieve this purpose - their size and volumetric efficiency are a good match for the typical application using an SZPL3102A/3103A. Surface-mount MLCCs typically have low equivalent series resistance and inductance (ESR, ESL) relative to their capacitance and therefore their effects are ignored in order to simplify the following calculations. Given the broad applicability of the SZPL3102A/3103A, take into consideration all the following constraints and select appropriate capacitance that meets all the applicable calculated minimums, considering component, bias, and environmental variables.

If the output voltage ripple (output inductor current induced) needs to be contained within given limits, use Equation *(3)* to approximate the required output capacitance to meet this requirement.

$$C_{OUT\_min} = \frac{V_{OUT} - \frac{V_{OUT}^2}{V_{IN}}}{8 \cdot F_{SW}^2 \cdot L_{OUT} \cdot V_{OUT\_rpl}} \quad (3)$$

Where:

- V_{OUT_rpl} is the peak-to-peak output voltage ripple target
- L_{OUT} is the output filter inductance
- V_{OUT} is the DC output voltage setpoint
- V_{IN} is the converter input voltage

If the converter powers a highly dynamic load, the “load apply” and “load remove” events are likely to lead to much higher amplitude, temporary output deviations from the DC setpoint. Immediately following a sudden load increase, the output will sag as the load energy is delivered from the charge stored in the output capacitors. The PWM controller senses this negative excursion and increases the duty cycle. The current ramps up in the inductor to compensate for the load increase and to replace the lost output charge. As equilibrium is reached, the PWM duty cycle is returned to the DC operating point. The delay through the feedback loop is dependent on several variables and not easily quantified for general purpose use inside a mathematical equation. An empirical time delay is used in place of a loop response time. The response time can be optimized for a set of operating conditions. In a wide-output application, such as USB-PD, where the PWM duty cycle can vary over a wide range, the response time changes in proportionality to the duty cycle. Use Equation *(4)* to estimate minimum output capacitance for a given load application output deviation.

$$C_{OUT\_min} = \frac{N \cdot I_{OUT\_step}}{2 \cdot F_{SW} \cdot V_{OUT\_uv}} \quad (4)$$

Where:

- V_{OUT_uv} is the allowed output voltage sag
- I_{OUT_step} is the load step magnitude
- F_{SW} is the converter switching frequency
- N is the empirical variable (~3 for D = 20 %, up to ~13 for D = 85 %)

For the case of a fast load removal, the inductor current previously sunk by the output load is absorbed by the output capacitor bank. In a complementary fashion to load the application, the increase in output voltage is sensed by the PWM controller, which in turn reduces the duty cycle. The inductor current is driven slightly negative, removing excess output charge and restoring the DC setpoint. Assuming instantaneous load removal and controller response immediately driving the duty cycle to 0, Equation ***Error! Reference source not found.Error! Reference source not found.*** can be used to calculate the necessary output capacitance to absorb the inductor stored energy.

$$C_{OUT\_min} = \frac{L \cdot \left(I_{OUT\_high}^2 - I_{OUT\_low}^2\right)}{V_{OUT\_ov}^2 + 2 \cdot V_{OUT} \cdot V_{OUT\_ov}} \quad (5)$$

Where:

- I_{OUT_high} is the load value before step down
- I_{OUT_low} is the load value at the end of step down
- V_{OUT_ov} is the allowed output voltage rise

Use the offered guidance above to establish a ‘floor’ for the minimum output capacitance (C_{OUT}) required. Finite component parasitics (ESR, ESL), including printed circuit board contributions, along with PWM controller architecture and feedback control design, can all affect the results and require additional decoupling.

Setting the Output Voltage

The output voltage is set via a resistor divider, part of the feedback compensation network connected to the feedback (FB) pin - refer to Figure 7. Choose R4 in a range of 5 kΩ to 100 kΩ, then use Equation *(6)* to calculate the value of R1 that yields the desired output voltage.

$$R1 = R4 \cdot \frac{V_{OUT} - V_{REF}}{V_{REF}} \quad (6)$$

Where:

- V_{REF} is the device reference voltage (~1.25 V)
- V_{OUT} is the desired output voltage
- R4 is a user-chosen resistance value

Closed-Loop Frequency Compensation

The typical SZPL3102A/3103A application is likely to employ a relatively small output filter, comprised mostly of ceramic capacitors. Given the ceramics' low equivalent series resistance, the filter requires more frequency compensation network design flexibility, prompting the need for user-adjustable external components. Figure 7 exemplifies a typical type-3 network used for this purpose.

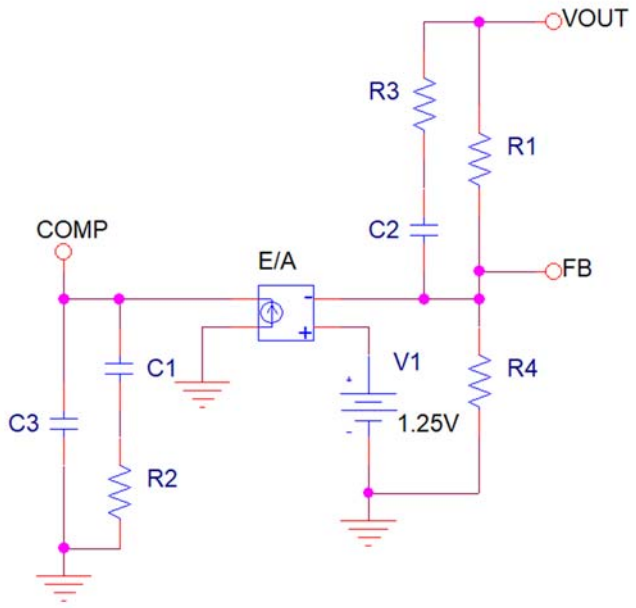


Figure 7: Type-3 Compensation Feedback Network

The circuit's closed loop operation can be represented by a couple of functional blocks: the modulator and the feedback network. The modulator is comprised of the PWM signal generation circuitry, a power stage, and an output filter. The feedback network is made up of the components shown in Figure 7. These blocks, working in tandem, regulate the output voltage and provide stable operation in response to input voltage, output voltage, and output load changes. Equations *(7)* through *(10)* describe the frequency response of the system while operating in CCM.

$$G_{CL}(\mathrm{f}) = G_{MOD}(\mathrm{f}) \cdot G_{FB}(f) \quad (7)$$

$$G_{MOD}(\mathrm{f}) = 14 \cdot \frac{1 + \mathrm{s(f)} \cdot \mathrm{ESR} \cdot C_{OUT}}{1 + \mathrm{s(f)} \cdot (\mathrm{ESR} + \mathrm{DCR}) \cdot C_{OUT} + s^2(f) \cdot L_{OUT} \cdot C_{OUT}} \quad (8)$$

$$G_{FB}(\mathrm{f}) = \frac{G_0 \cdot R4}{\mathrm{R1} + \mathrm{R4}} \cdot \frac{1 + \mathrm{s(f)} \cdot (\mathrm{R1} + \mathrm{R3}) \cdot \mathrm{C2}}{1 + \mathrm{s(f)} \cdot \left(\frac{R1 \cdot R4}{R1 + R4} + \mathrm{R3}\right) \cdot \mathrm{C2}} \cdot \frac{1 + s(f) \cdot R2 \cdot C1}{1 - C1 \cdot C3 \cdot R2 \cdot r0 + s(f) \cdot [r0 \cdot (C1 + C3) + R2 \cdot C1]} \quad (9)$$

$$\mathrm{s(f)} = 2 \cdot \pi \cdot \mathrm{f} \cdot \mathrm{j} \quad (10)$$

Where:

- G_{CL}, G_{MOD}, G_{FB} are the closed-loop, modulator and feedback gains, respectively
- C_{OUT} and ESR are the output capacitor bank's total capacitance and ESR
- L_{OUT} and DCR are the output of inductor's inductance and DC resistance
- G_0 is the transconductance error amplifier's DC gain, typically 1000 (1e3)
- r_0 is the transconductance error amplifier's output resistance, typically 10MΩ (1e7)
- R1, R2, R3, R4, C1, C2, C3 are the feedback network components, as shown in Figure 7

The output filter shapes the modulator frequency response with a double-pole break frequency at F_{LC} and a zero at F_{CE}.

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}} \quad (11)$$

$$F_{CE} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad (12)$$

The recommended typical loop compensation design should aim for a closed-loop bandwidth (cross-over frequency, F_{CO}, where $F_{CO} > F_{LC}$) less than 100kHz, user-selected in the 20 kHz to 70 kHz range. C3 and R3 components can be omitted from the design (connect C2 to V_{OUT}), allowing the feedback response to roll off at very high frequencies with the natural response of the error amplifier. With R1 and R4 already calculated from setting the output voltage, calculate R2, C1, and C2 according to Equations *(1)* through *(15)*.

$$R2 = \frac{F_{CO} \cdot R1 \cdot 1.5}{14 \cdot F_{LC}} \quad (13)$$

$$C1 = \frac{1}{2 \cdot \pi \cdot R2 \cdot 0.1 \cdot F_{LC}} \quad (14)$$

$$C2 = \frac{1}{2 \cdot \pi \cdot R1 \cdot [0.3 \cdot (F_{CO} - F_{LC}) + F_{LC}]} \quad (15)$$

To verify the response meets the intended design goals, it is recommended that a mathematical model or a simulation tool be used to visualize the feedback network design prior to implementation.

DCM operation response does not adhere as closely to the previously described mathematical loop response. Nonetheless, operation in DCM is stable and commensurate with CCM performance.

Typical Application Diagrams

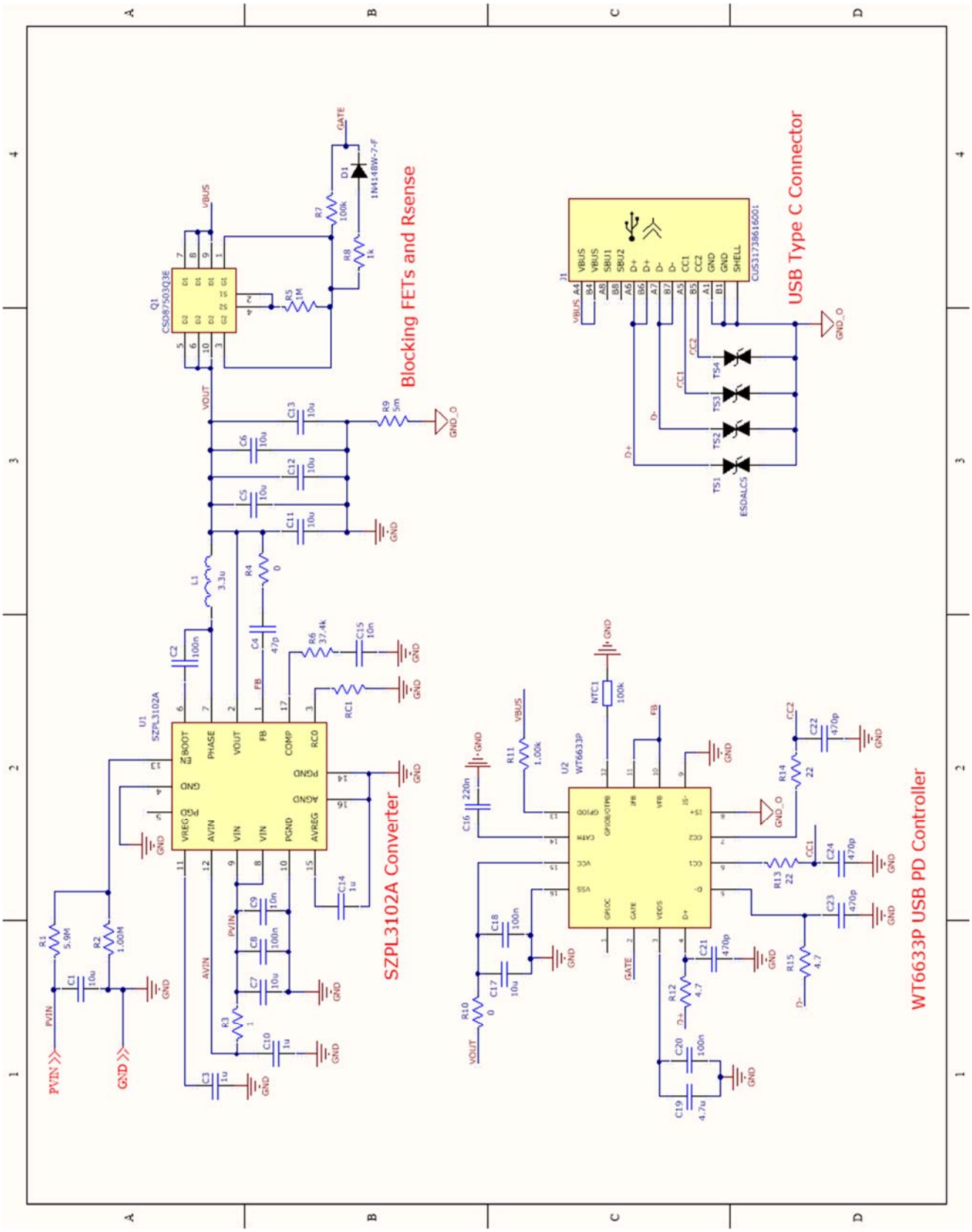


Figure 8: Typical Schematic with a WT6633P PD Controller

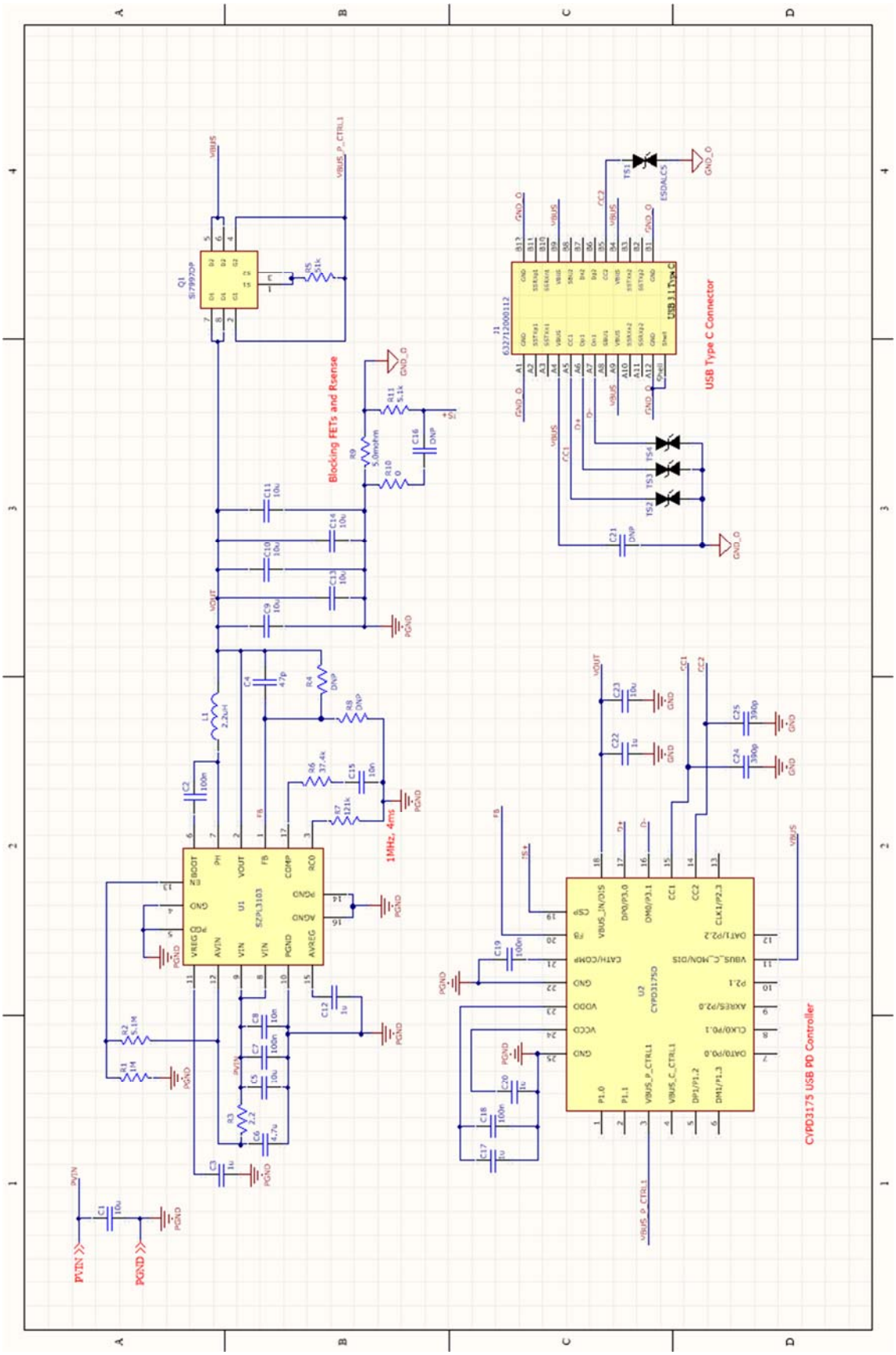


Figure 9 Typical Schematic with Cypress CYPD3175 PD Controller

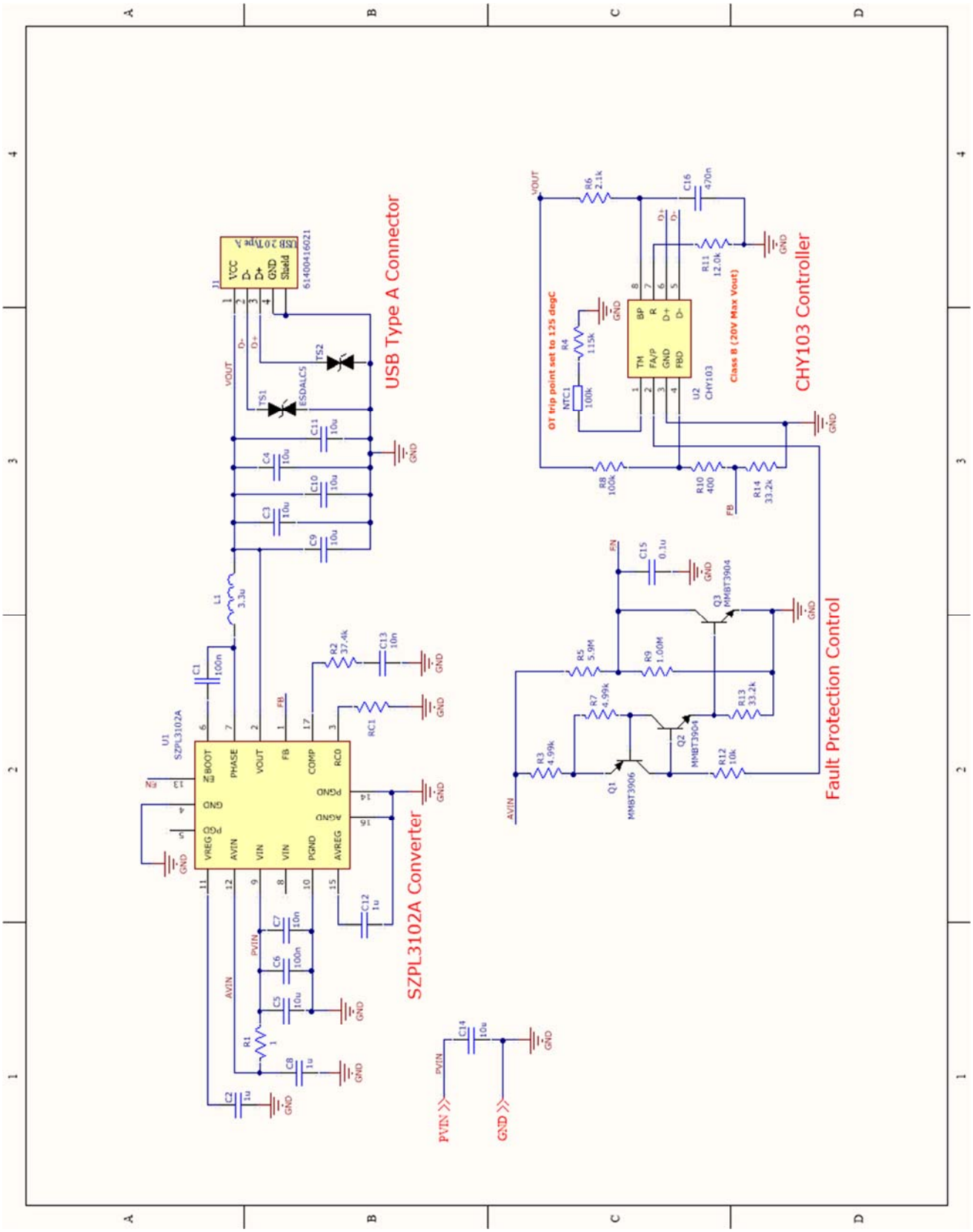


Figure 10 Typical Schematic with a CHY103 Quick Charge Controller

Product Ordering Information

Part Number	Package	Description
SZPL3102A-CF33	QFN (3 mm x 3 mm)	Integrated, Wide Voltage, Buck Converter with Momentary Feedback Divider
SZPL3103A-CF33	QFN (3 mm x 3 mm)	Integrated, Wide Voltage, Point of Load Buck Converter

Product Image

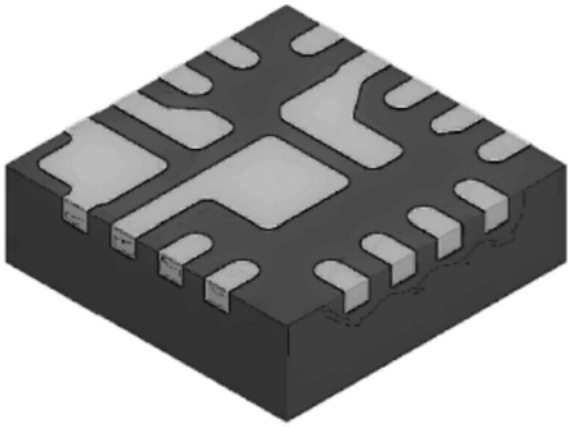
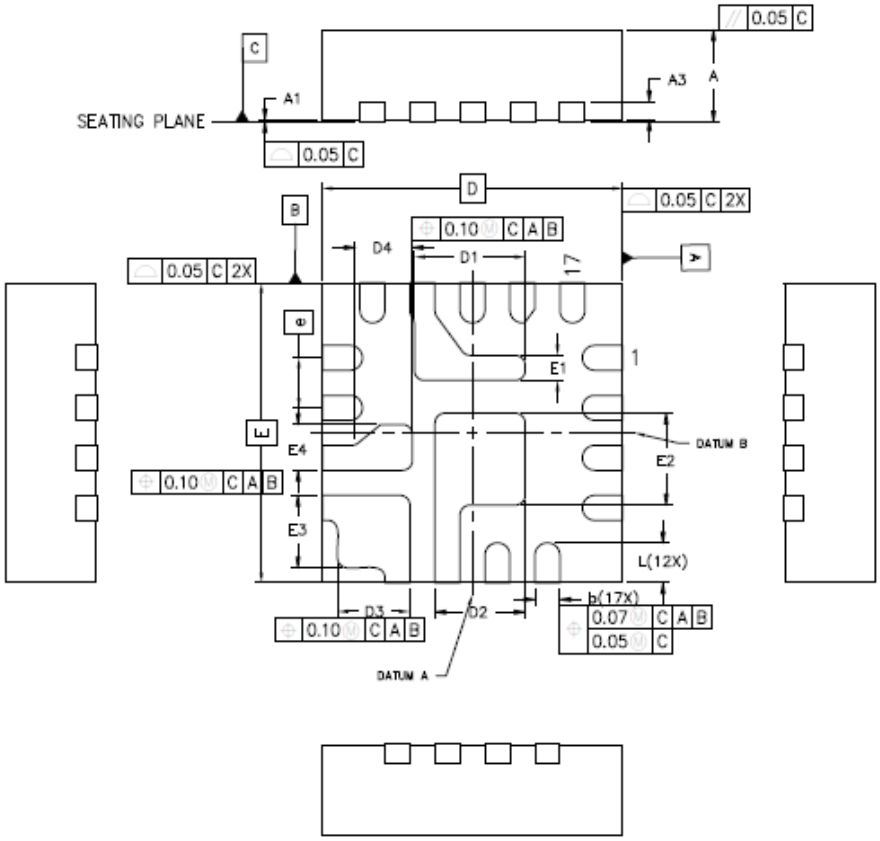


Figure 11: SZPL3102A/3103A Product Image

Package Dimensions



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D1	1.01	1.11	1.21
E1	0.15	0.25	0.35
D2	0.80	0.90	1.00
E2	0.82	0.92	1.02
D3	0.63	0.73	0.83
E3	0.63	0.73	0.83
D4	0.47	0.57	0.67
E4	0.36	0.46	0.56
e		0.50 BSC	
L	0.30	0.40	0.50
N		17	

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5–2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pads as well as the terminals

Figure 12: Package Dimensions

Recommended PCB Footprint

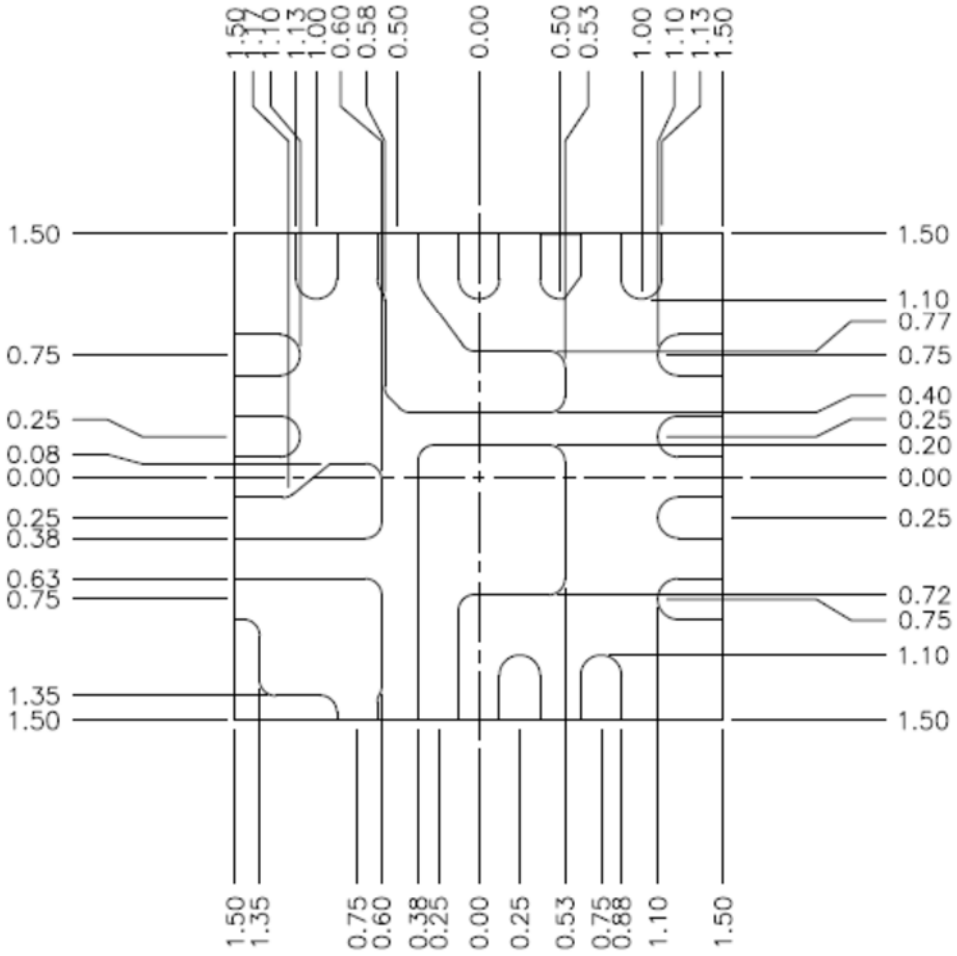


Figure 13: Recommended PCB Footprint

Revision History

Revision	Date	Author	Note
1.0	Sep 16, 2020	TW	Initial Release.
2.0	Nov 18, 2020	BD/TW	Updated specification values.

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