

P-Channel Enhancement Mode MOSFET

TDM3421

**DESCRIPTION**

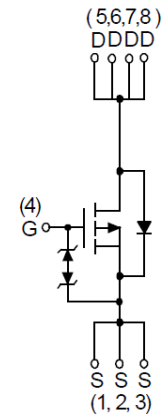
The TDM3421 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

**GENERAL FEATURES**

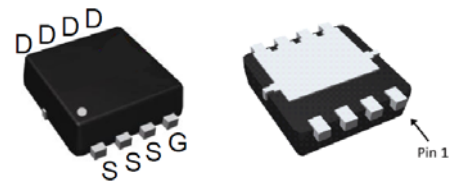
- RDS(ON) < 32mΩ @ VGS=-4.5V  
RDS(ON) < 19mΩ @ VGS=-10V
- Reliable and Rugged
- ESD protection pass 2KV
- Lead free product is available
- PPAK-3\*3-8 Package

**Application**

- PWM applications
- Load switch
- Power management



P-Channel MOSFET



PPAK-3\*3-8

**ABSOLUTE MAXIMUM RATINGS**(*TA=25°C unless otherwise noted*)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±25	V
Diode Continuous Forward Current	I <sub>S</sub> (T <sub>C</sub> =25 °C)	-16	A
Pulsed Drain Current	I <sub>DM</sub> (T <sub>C</sub> =25 °C)	-70	A
Continuous Drain Current	I <sub>D</sub> (T <sub>C</sub> =25 °C)	-32	A
	I <sub>D</sub> (T <sub>C</sub> =100 °C)	-20	A
Maximum Power Dissipation	P <sub>D</sub> (T <sub>C</sub> =25 °C)	29.8	W
	P <sub>D</sub> (T <sub>C</sub> =100 °C)	11.9	W
Continuous Drain Current	I <sub>D</sub> (T <sub>A</sub> =25 °C)	-10.5	A
	I <sub>D</sub> (T <sub>A</sub> =70 °C)	-8.4	A
Maximum Power Dissipation (note1)	P <sub>D</sub> (T <sub>A</sub> =25 °C)	3.1	W
	P <sub>D</sub> (T <sub>A</sub> =70 °C)	2	W
Maximum Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to 150	°C
Thermal Resistance-Junction to Ambient (note1)	RθJA(t≤10s)	40	°C/W
	RθJA(Steady State)	75	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>STATIC CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
<b>ON CHARACTERISTICS</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.3	-1.8	-2.3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_{DS}=-8.2A$	-	25	32	m $\Omega$
		$V_{GS}=-10V, I_{DS}=-10.5A$	-	16	19	m $\Omega$
<b>DYNAMIC CHARACTERISTICS</b> (Note 4)						
Gate Resistance	$R_g$	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	4	-	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V, F=1.0MHz$	-	999	-	PF
Output Capacitance	$C_{oss}$		-	220	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	170	-	PF
<b>SWITCHING CHARACTERISTICS</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega, V_{GEN}=-10V, R_G=6\Omega, I_{DS}=-1A$	-	11.2	-	nS
Turn-on Rise Time	$t_r$		-	10.6	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	37	-	nS
Turn-Off Fall Time	$t_f$		-	50	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_{DS}=-10.5A, V_{GS}=-10V$	-	20	-	nC
Gate-Source Charge	$Q_{gs}$		-	1.1	-	nC
Gate-Drain Charge	$Q_{gd}$		-	7.7	-	nC
Body Diode Reverse Recovery Time	$T_{rr}$	$I_{DS}=-10.5A, di/dt=100A/\mu s$	-	18	-	nS
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	9	-	nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_{SD}=-1A$	-	-0.7	-1	V

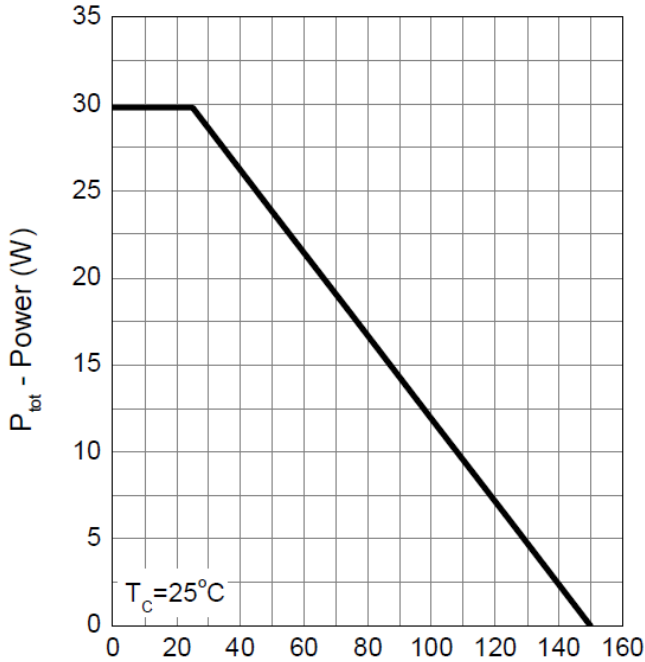
**NOTES:**

- Surface Mounted on  $1in^2$  pad area,  $t_s \leq 10sec$ .  $R_{\theta JA}$  steady state  $t = 999s$ .
- The power dissipation  $P_D$  is based on  $T_{J(MAX)} = 150^{\circ}\text{C}$ , and it is useful for reducing junction-to-case thermal resistance ( $R_{\theta JC}$ ) when additional heat sink is used.
- Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing

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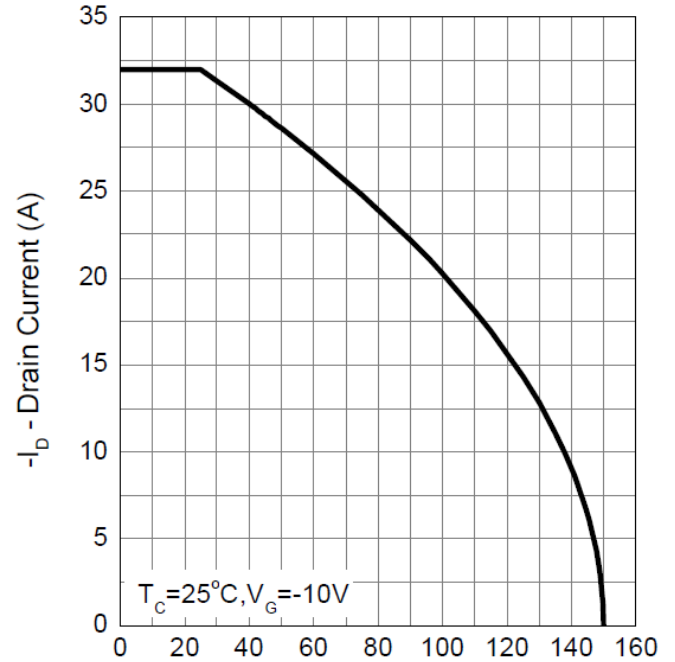
Typical Operating Characteristics

Power Dissipation



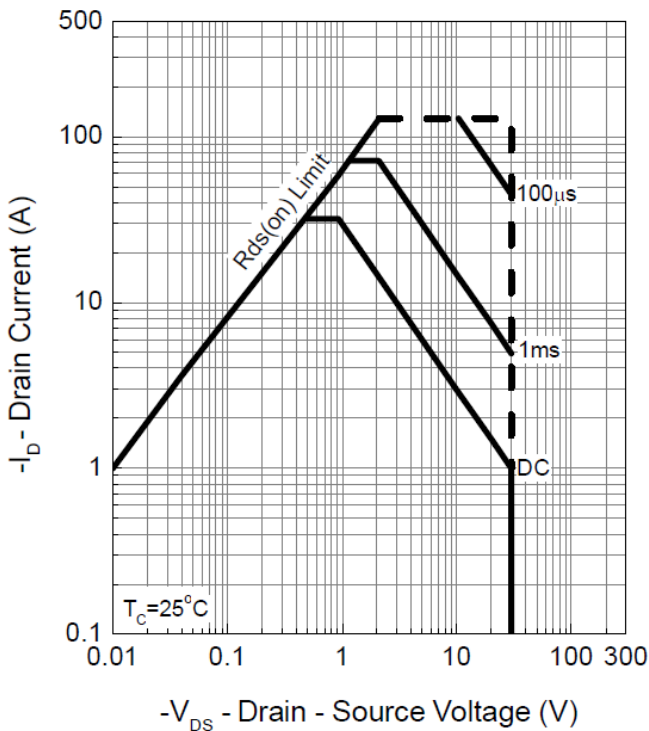
$T_j$  - Junction Temperature ( $^{\circ}\text{C}$ )

Drain Current

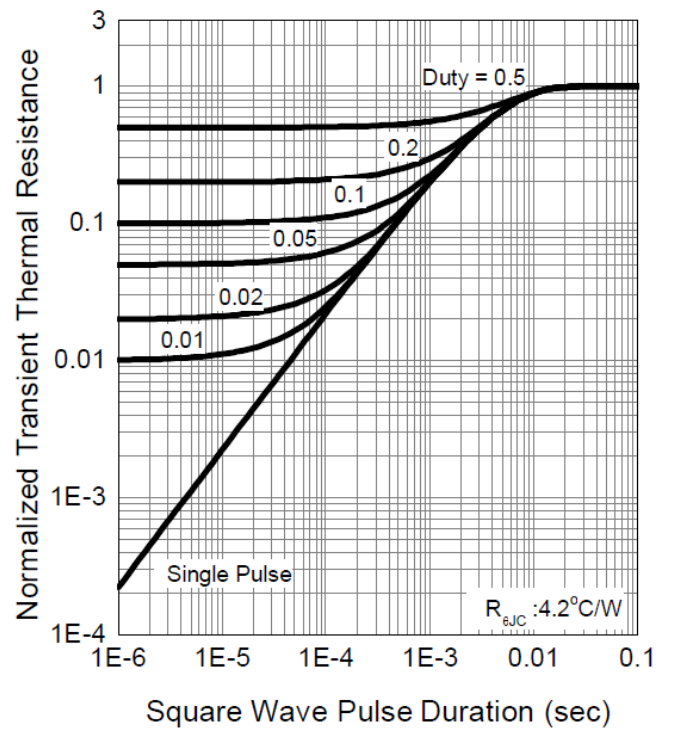


$T_j$  - Junction Temperature ( $^{\circ}\text{C}$ )

Safe Operation Area

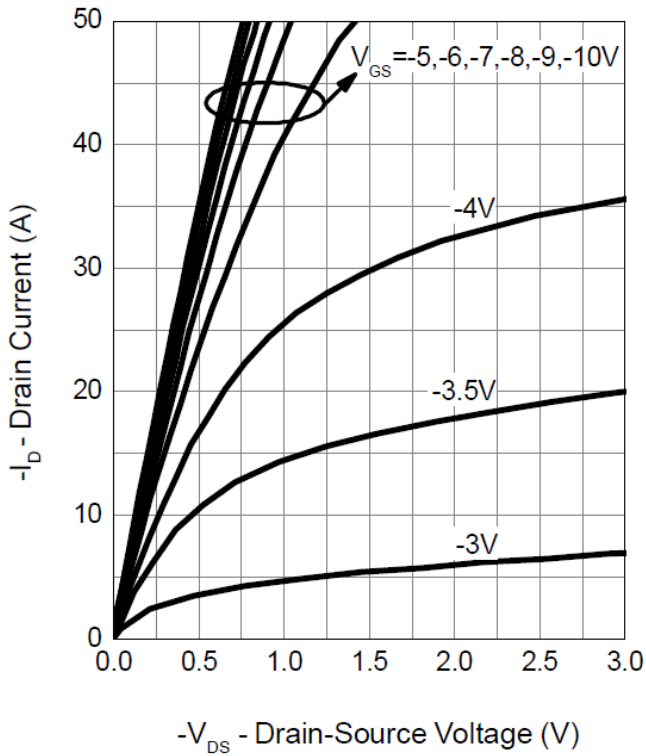


Thermal Transient Impedance

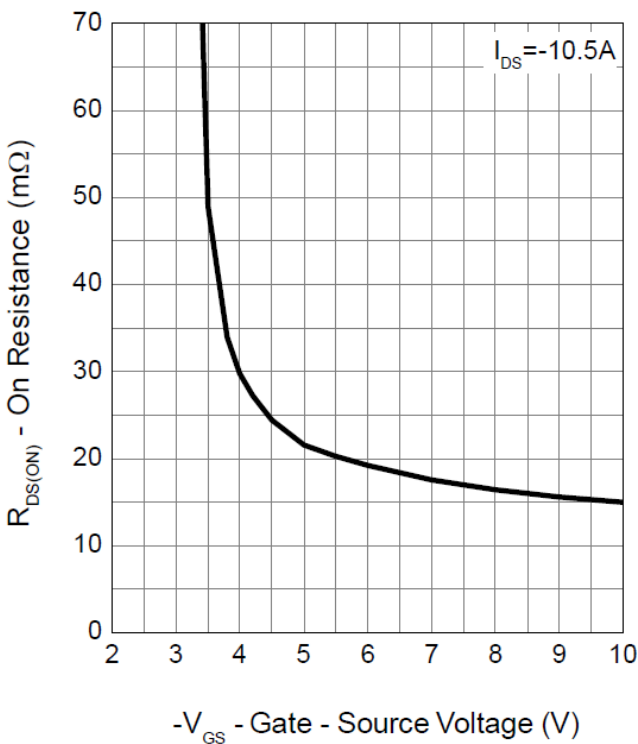


Typical Operating Characteristics(Cont.)

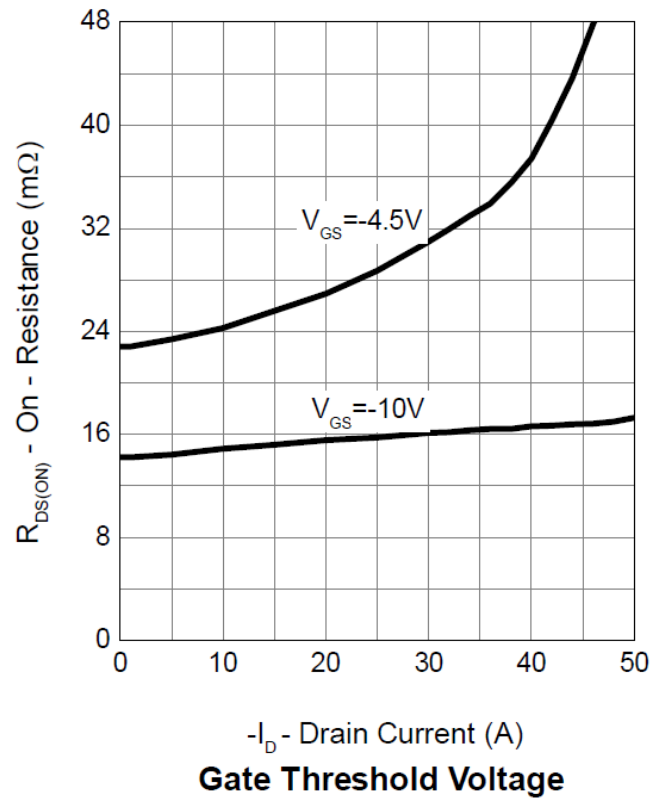
Output Characteristics



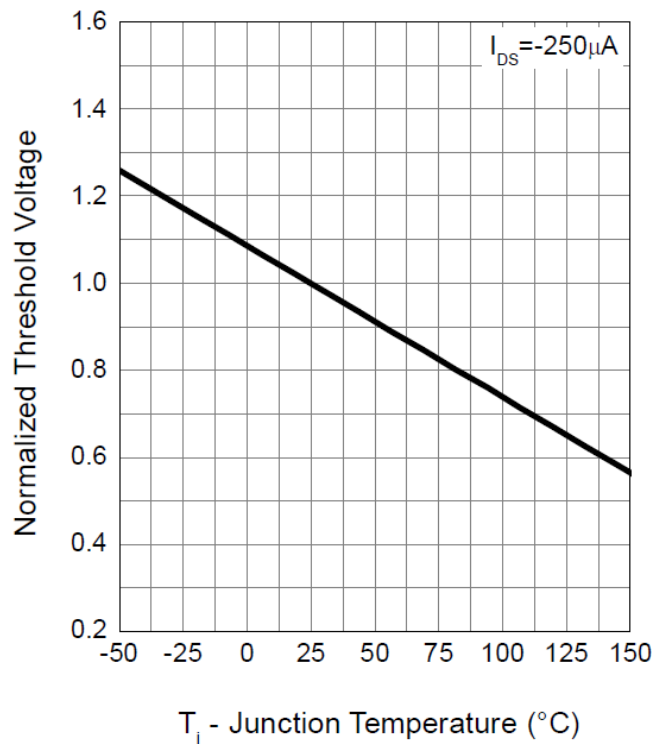
Gate-Source On Resistance



Drain-Source On Resistance

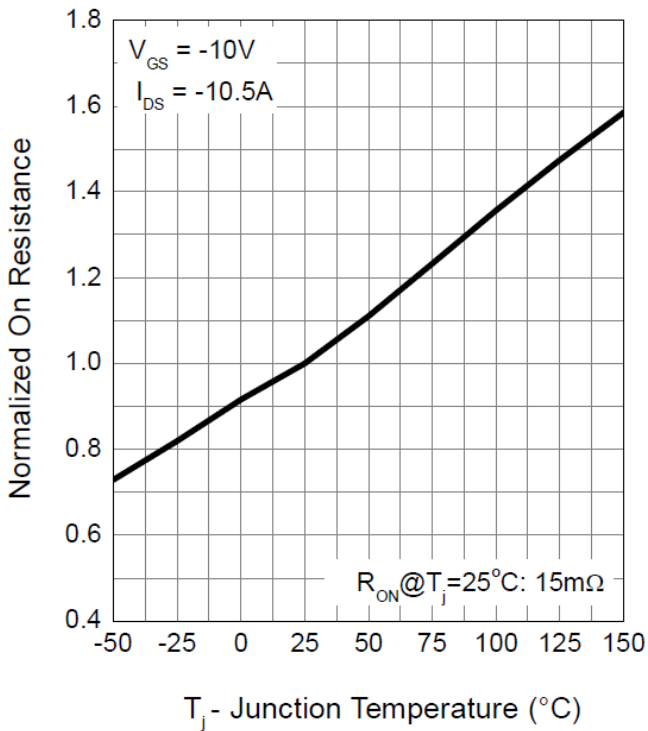


Gate Threshold Voltage

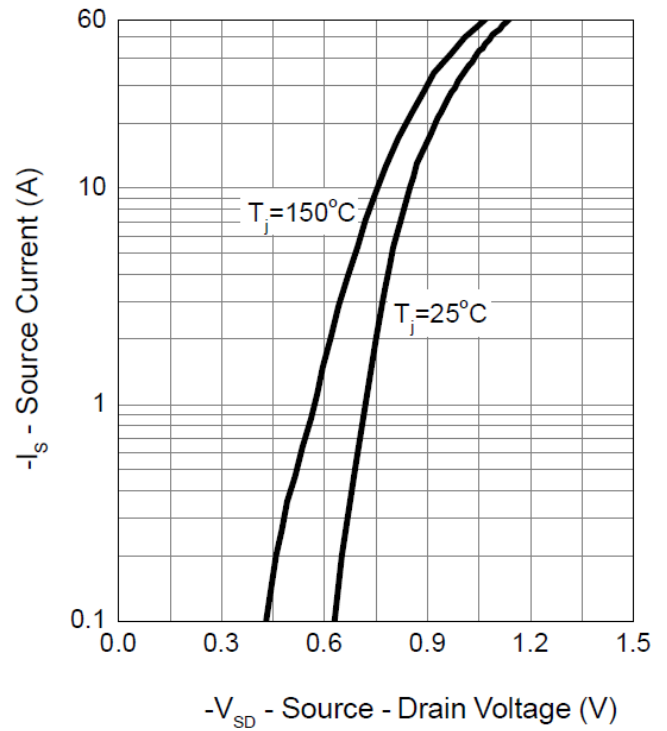


Typical Operating Characteristics (Cont.)

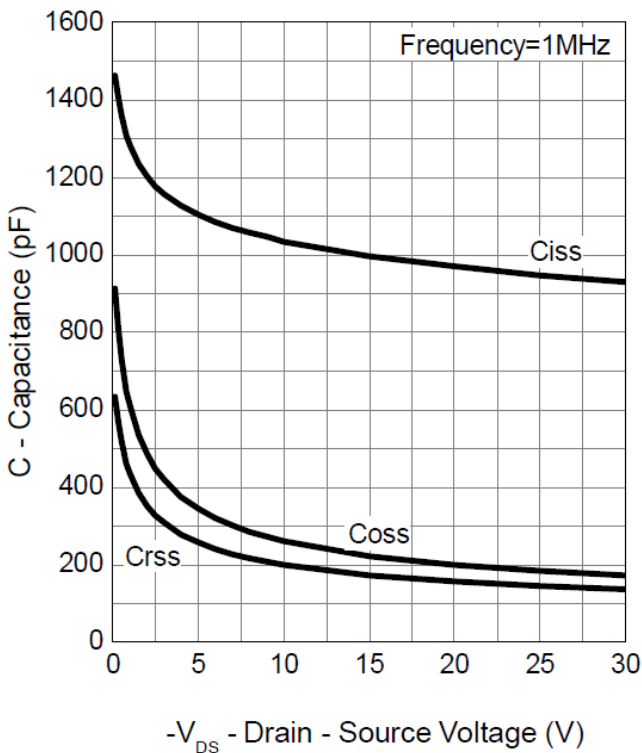
Drain-Source On Resistance



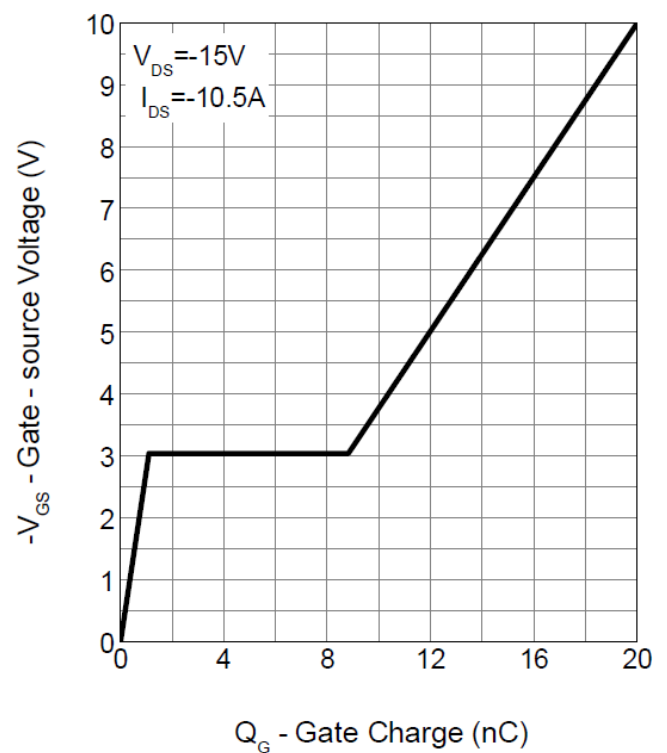
Source-Drain Diode Forward



Capacitance

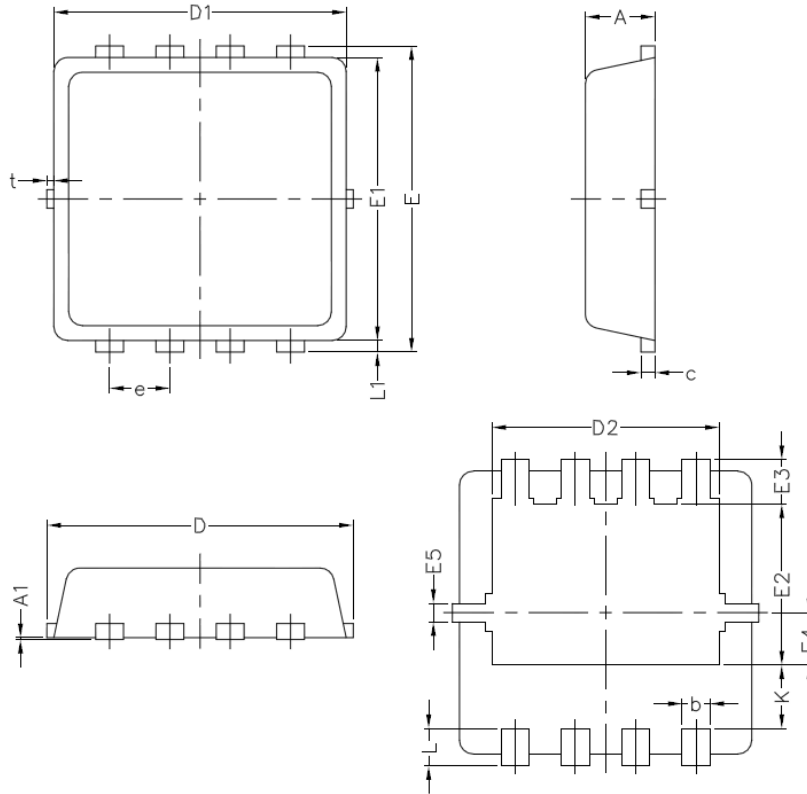


Gate Charge



Package Information

PPAK-3\*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes