

P-Channel Enhancement Mode MOSFET

TDM3205

DESCRIPTION

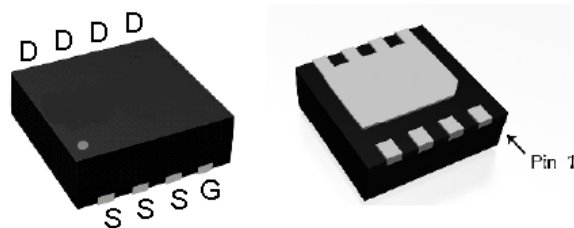
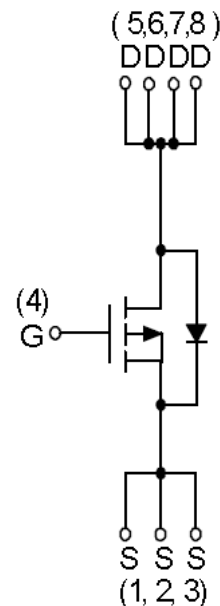
The TDM3205 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

- RDS(ON) < 9.9mΩ @ VGS=-1.8V
RDS(ON) < 6.8mΩ @ VGS=-2.5V
RDS(ON) < 4.5mΩ @ VGS=-4.5V
RDS(ON) < 3.5mΩ @ VGS=-10V
- High Power and current handing capability
- Surface Mount Package
- Lead Free and Green Devices Available(RoHS Compliant)

Application

- PWM applications
- Load switch
- Power management
- Powered Systems



ABSOLUTE MAXIMUM RATINGS(TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current @ Continuous	I _D (TA=25°C)	-25	A
	I _D (TA=70°C)	-20	A
Drain Current @ Current-Pulsed (Note 1)	I _{DM} (Tc=25°C)	-95	A
Maximum Power Dissipation (TA=25°C)	P _D	4.2	W
Maximum Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Ambient (Note 2)	R _{θJA}	70	°C/W
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ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.7	-0.9	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-1.8V, I_D=-10A$		6.8	9.9	m Ω
		$V_{GS}=-2.5V, I_D=-20A$		4.8	6.8	m Ω
		$V_{GS}=-4.5V, I_D=-20A$		3.5	4.5	
		$V_{GS}=-10V, I_D=-20A$		2.9	3.5	m Ω
DYNAMIC CHARACTERISTICS (Note3)						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, F=1.0MHz$		5350		PF
Output Capacitance	C_{oss}			1020		PF
Reverse Transfer Capacitance	C_{rss}			810		PF
SWITCHING CHARACTERISTICS (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=10V, R_L=10\Omega, V_{GEN}=-4.5V,$ $R_G=6\Omega, I_D=-1A$		19		nS
Turn-on Rise Time	t_r			25		nS
Turn-Off Delay Time	$t_{d(off)}$			228		nS
Turn-Off Fall Time	t_f			72		nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=-20A, V_{GS}=-4.5V$		54		nC
Gate-Source Charge	Q_{gs}			4.1		nC
Gate-Drain Charge	Q_{gd}			17		nC
Body Diode Reverse Recovery Time	T_{rr}	$I_F=-20A, di/dt=100A/\mu s$		33		nS
Body Diode Reverse Recovery Charge	Q_{rr}			17		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 2)	V_{SD}	$V_{GS}=0V, I_S=1A$		-0.5	-1	V

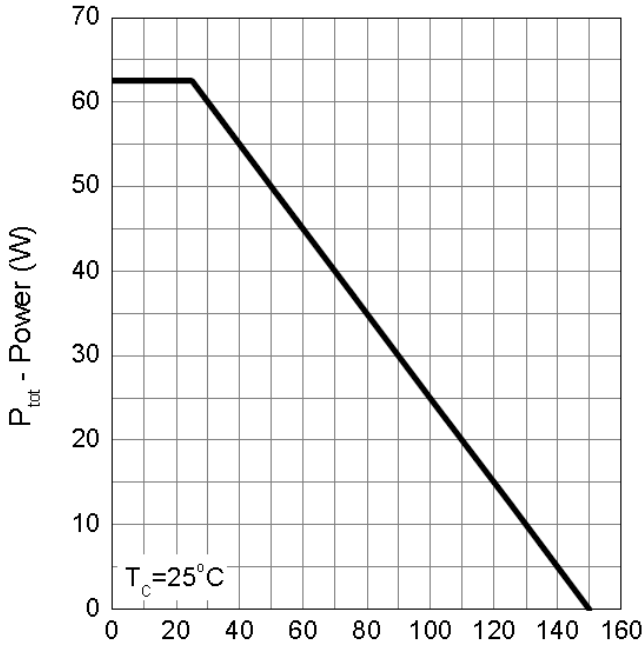
NOTES:

1. Pulse width limited by max. junction temperature.
2. $R_{\theta JA}$ steady state=999s. $R_{\theta JA}$ is measured with the device mounted on 1in2, Fr-4 board with 2oz.Copper
3. Guaranteed by design, not subject to production testing

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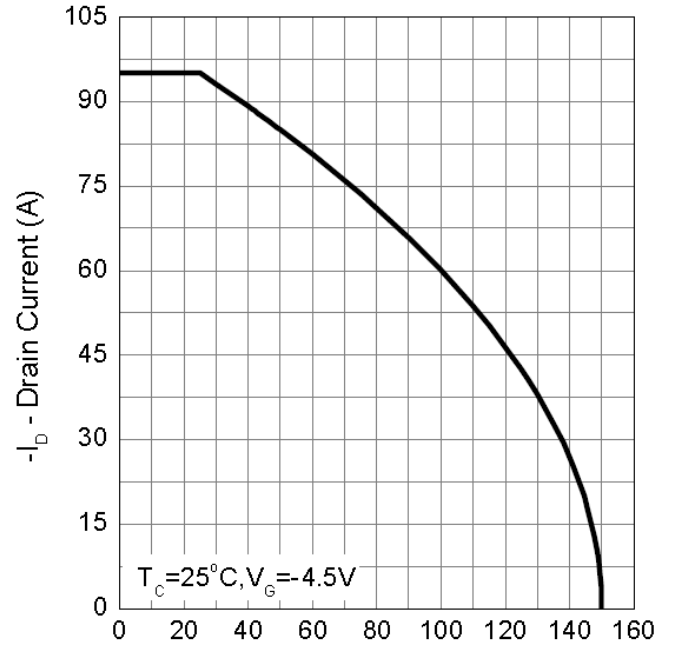
Typical Operating Characteristics

Power Dissipation



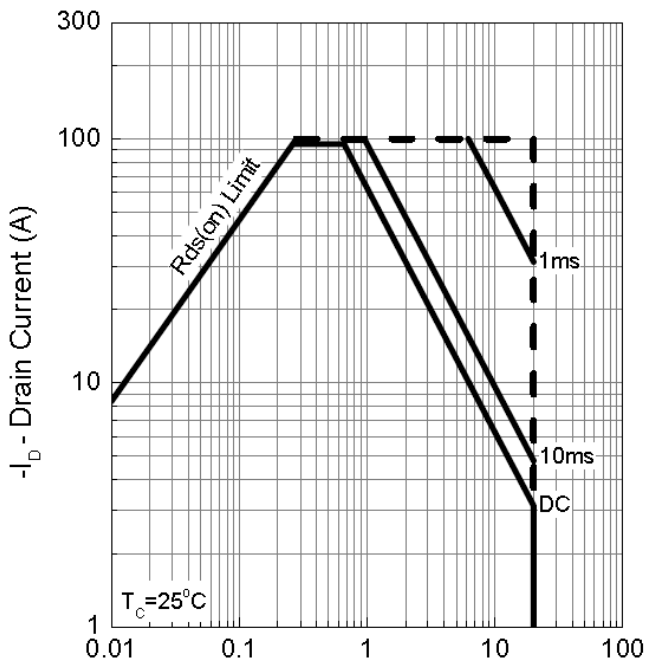
T_j - Junction Temperature (°C)

Drain Current



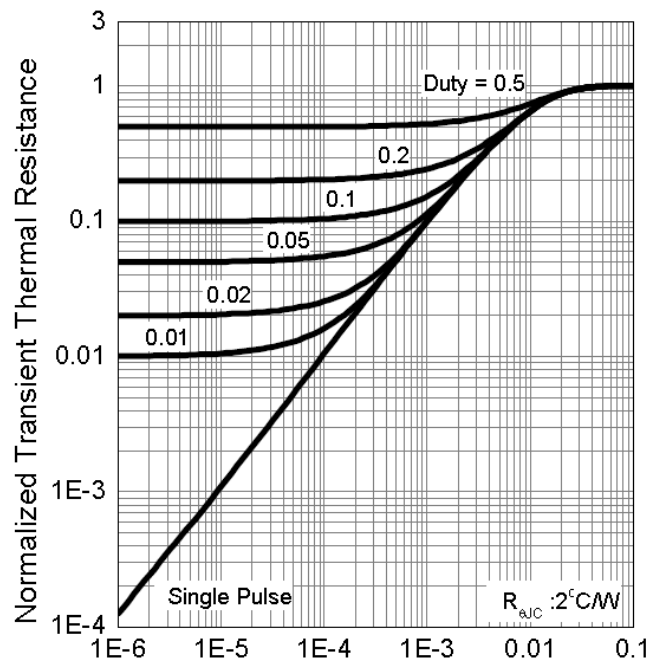
T_j - Junction Temperature (°C)

Safe Operation Area



$-V_{DS}$ - Drain - Source Voltage (V)

Thermal Transient Impedance

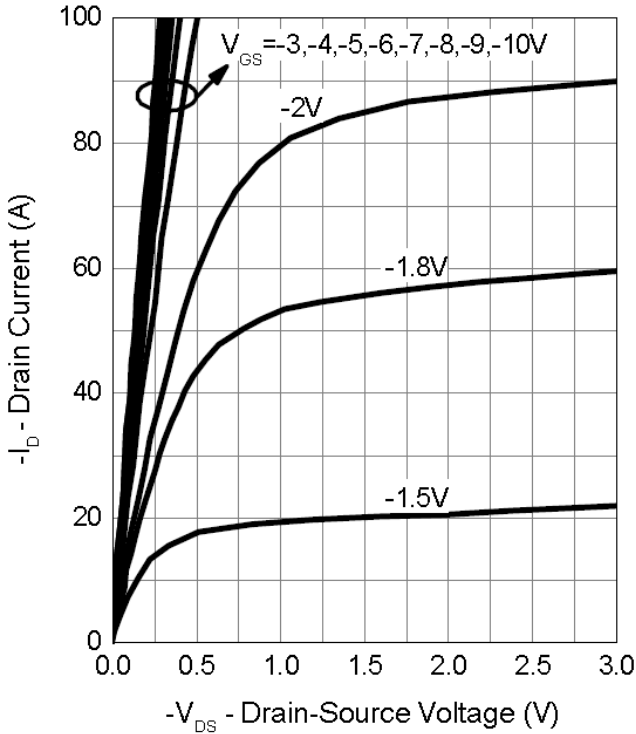


Square Wave Pulse Duration (sec)

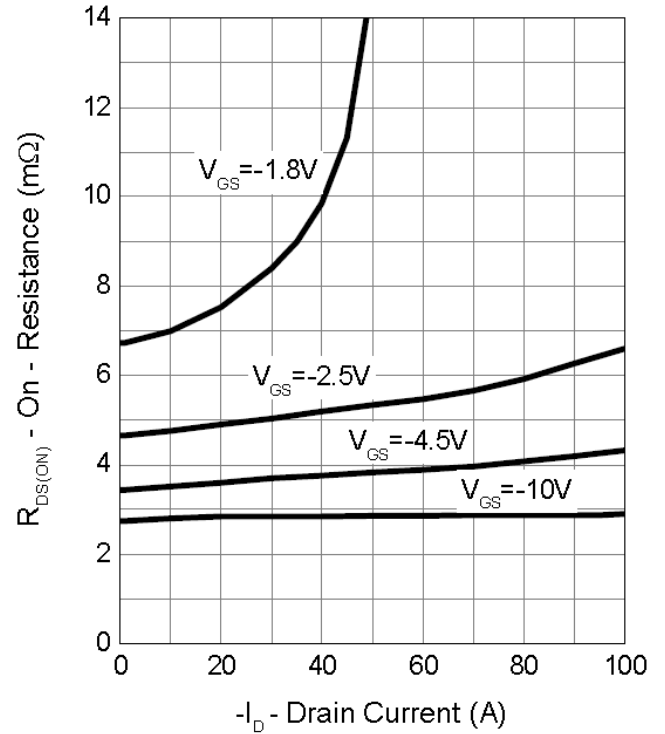
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Typical Operating Characteristics(Cont.)

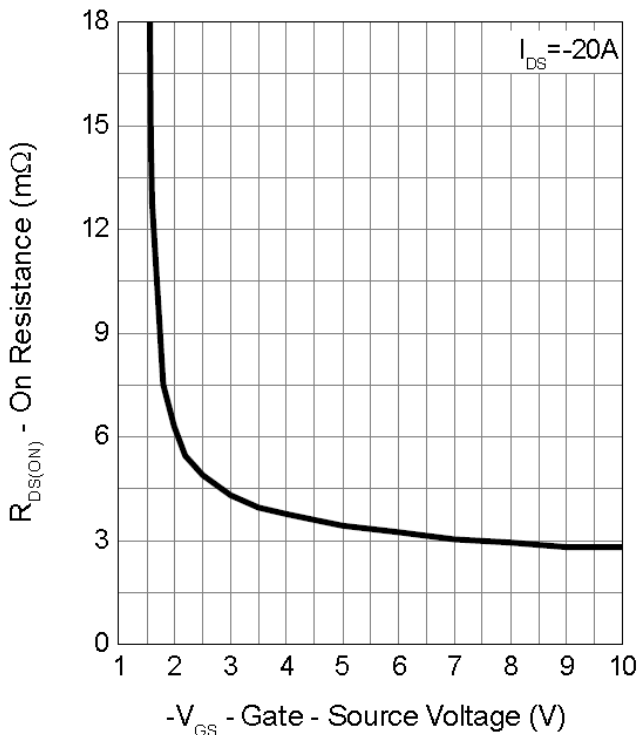
Output Characteristics



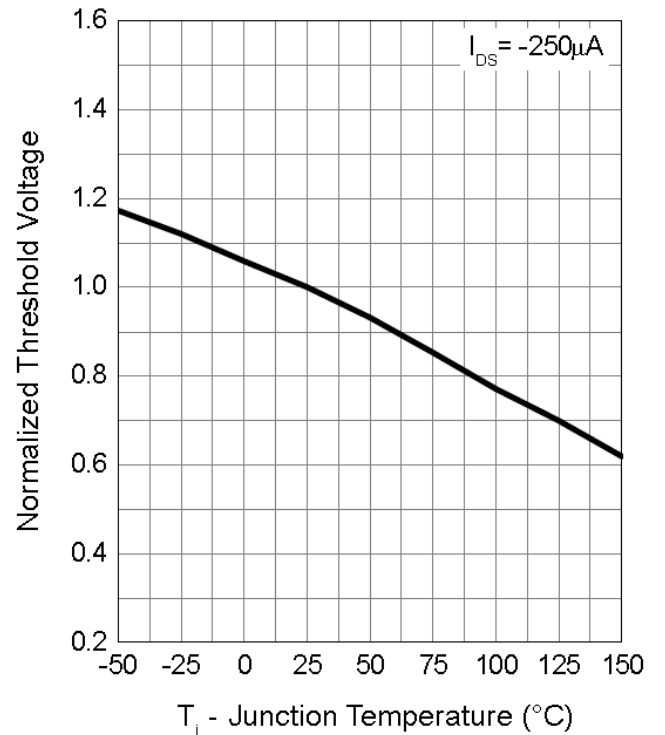
Drain-Source On Resistance



Gate-Source On Resistance



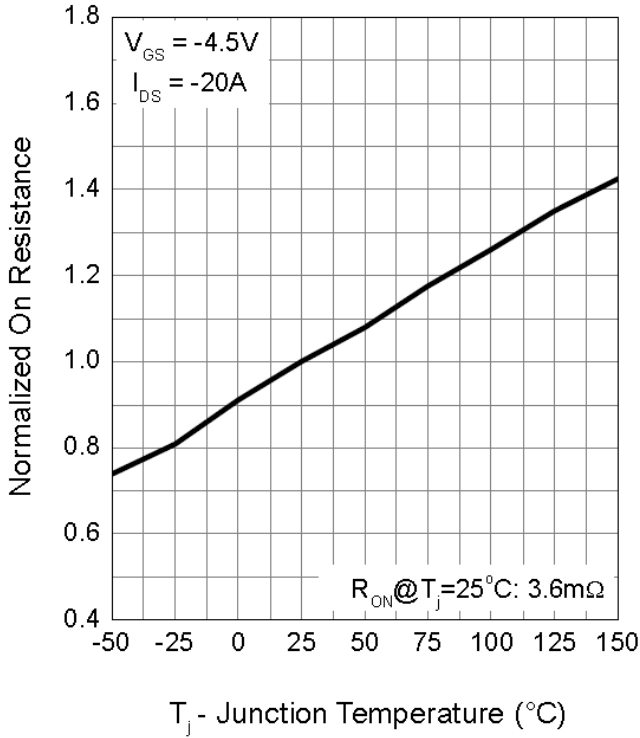
Gate Threshold Voltage



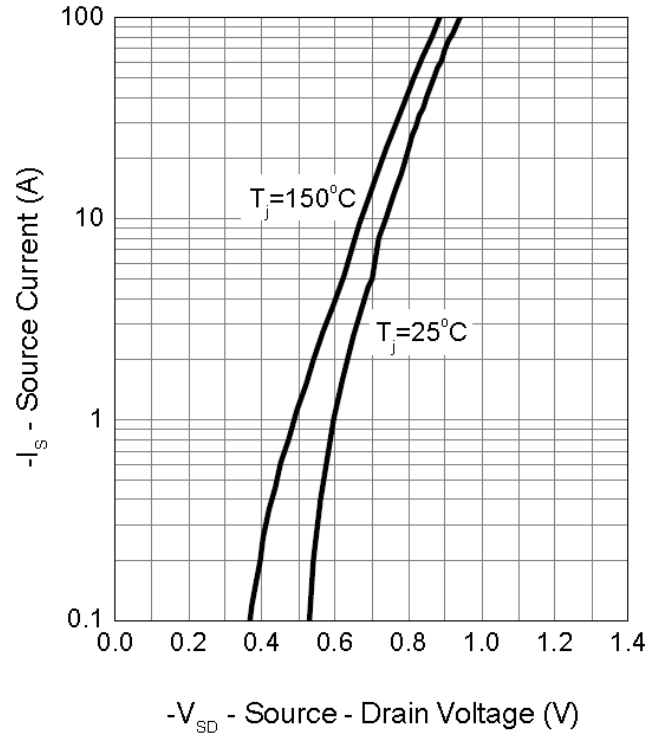
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Typical Operating Characteristics (Cont.)

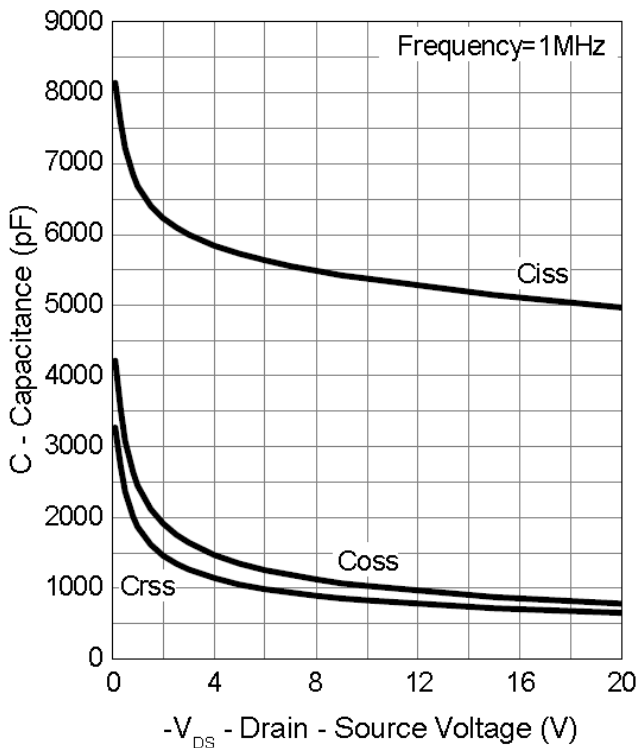
Drain-Source On Resistance



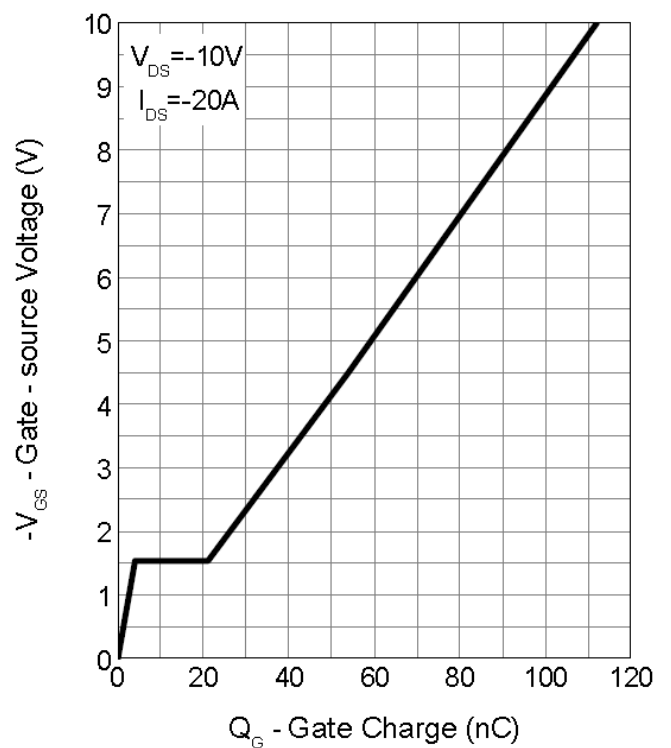
Source-Drain Diode Forward



Capacitance

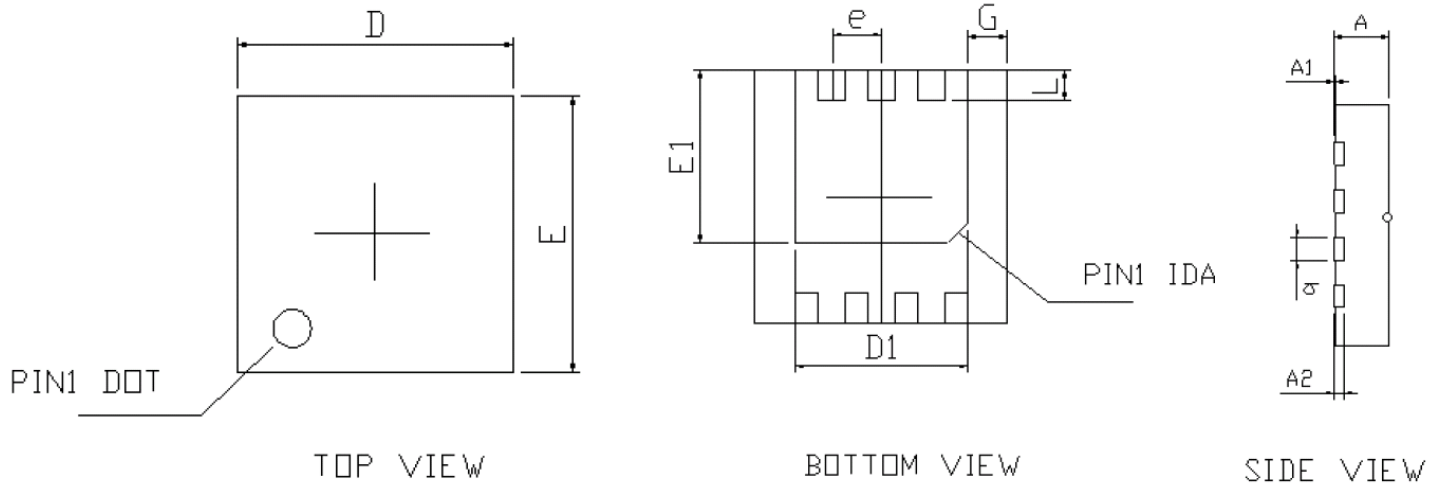


Gate Charge



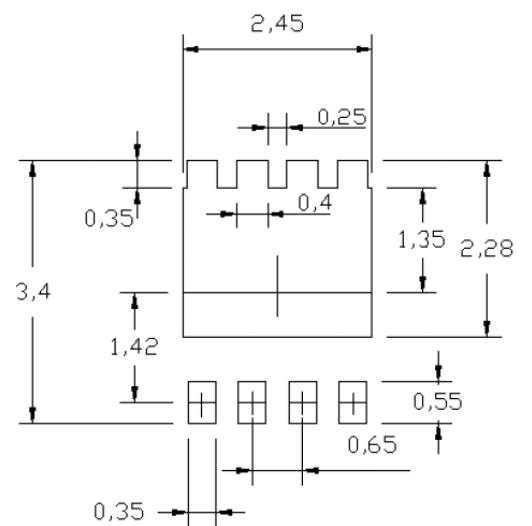
Package Information

DFN3.3*3.3-8 Package



SYMBOLS	DFN3.3x3.3B-8_EP1_S			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.032
A1	0.000	0.050	0.000	0.002
A2	0.100	0.250	0.004	0.010
b	0.240	0.350	0.009	0.014
D	3.150	3.400	0.124	0.134
D1	2.100	2.350	0.083	0.093
E	3.150	3.400	0.124	0.134
E1	2.150	2.350	0.850	0.093
e	0.600	0.700	0.024	0.028
G	0.475	0.575	0.019	0.023
L	0.350	0.450	0.014	0.018

RECOMMENDED LAND PATTERN



Design Notes